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Double Spacer LOCOS Process with Shallow Recess of Silicon for 0.20 μm Isolation

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Double spacer LOCOS process with shallow recess of silicon (DS-LOCOS), which is a simple and productive isolation technology for 0.20 μm design rule, is described. The process has two spacers, a thin nitride and a medium temperature CVD oxide (MTO), to the sidewall of pad oxide/nitride stack and uses some amount of overetchings to produce shallow recess of silicon substrate. The existence of MTO makes the silicon recess by spacer overetching easy and allows use of very thin spacer nitride while keeping enough offset length to compensate the bird's beak encroachment. It has been found that physical profiles and electrical properties mainly depend on the amount of overetchings in both isolation etching and spacer etching. DS-LOCOS achieved over 80% of field oxide volume ratio, superior planar surface, and no degradation in punchthrough voltage down to 0.20 μm isolation spacing.

I. INTRODUCTION

Silicon recess in LOCOS process becomes a popular technique in recent isolation technology to improve oxide volume ratio, surface planarity, and isolation ability [1,2,3]. However, a simple addition of silicon recess to conventional LOCOS structure causes larger bird's beak due to lateral oxidation through the sidewall of the recessed substrate. Thus, the use of spacers at the pad oxide/nitride stack edge to give offset and lateral sealing is inevitable to prevent bird's beak encroachment as long as silicon substrate is recessed [2,4]. In the view of the sealing of oxidant diffusion, nitride is the best material [5,6]. But, the use of thick nitride spacer to give enough offset length causes a significant stress to the silicon substrate. On the other hand, as device dimension shrinks to sub-quarter micron range, the required field oxide thickness becomes thinner as well. This reduction of field oxide thickness makes deep recess of silicon substrate inessential.

With these considerations, we propose a new isolation process named as Double Spacer LOCOS (DS-LOCOS) which has two spacers and very shallow recess of silicon. The process does not have intentional silicon etching step but achieves the shallow recess of silicon through nitride overetching using the property that silicon etching rate during nitride etching is enhanced under the existence of oxygen.

II. DS-LOCOS PROCESS

A process sequence of the DS-LOCOS structure is illustrated in Fig. 1. A thin thermal oxide is first grown as the pad oxide and followed by LPCVD nitride deposition as the pad nitride. The isolation area is defined by photolithography process and followed by nitride etching (named isolation etching) with some amount of overetching to recess silicon substrate a little. After stripping photoresist, wafers are immersed into dilute HF solution to etch off the pad oxide completely in the open areas. A thin nitride and medium temperature CVD oxide (MTO) are deposited in due course. Second nitride etching (named spacer etching) to form spacer at the edge of pad oxide/nitride stack is followed using the same etching chemistry as the isolation etching, with the some amount of overetching as well. After removing spacer oxide by wet chemical, field oxidation is carried out. As the field oxidation proceeds, the thin spacer nitride is folded up as shown in Fig. 1(e), producing relatively low stress to the field oxide edge compared with the nitride single spacer structure. After removing pad nitride and spacer nitride, channel stop implantation is carried out through the field oxide.

Here, the silicon recess depth is mainly decided by amount of overetchings during both isolation etching and spacer etching. By controlling both overetchings we could achieve successful recess of silicon with the depth of 300 ~ 600 Å. MTO in this process plays very important roles. First, it allows use of very thin spacer nitride while keeping enough offset length to compensate the bird's beak encroachment. Second, it makes the silicon recess by spacer overetching easy because silicon etching rate during nitride etching is enhanced under the existence of oxygen produced from etched oxide film.

III. RESULTS AND DISCUSSION

Figure 2 shows field oxide profiles after gate cleaning at 0.20 μm isolation spacing when the field oxide thickness target in a wide open area is 3200 Å. Here, the pad oxide thickness was 150 Å, pad nitride 2000 Å, thin nitride spacer 100 Å, and MTO 200 Å.

Overetching percents in isolation etching were 50% for (a) and (b), and 100% for (c). Overetching percents in spacer etching were 170% for (a) and (c), and 230% for (b). Fig. 2(a) and (c) have similar bird's beak length of about 0.03 μm/side but (b) has longer bird's beak og 0.05 μm/side. For the oxide volume ratio, percentage of field oxide thickness under wafer surface *vs.* field oxide thickness, (c) has the highest value of about 90%. From this result, we could see that the bird's beak mainly depended on overetching percent in spacer etching, but the volume ratio depended on isolation etching. But in all cases, over 80% of volume ratio and superior planar surfaces were achieved. Higher overetching percent in isolation etching produced higher volume ratio but sharp corner at the field oxide edge as shown in Fig. 2(c), which resulted in larger junction leakage current as high as one order of magnitude compared with the cases of Fig. 2(a) or (b).

Figure 3 shows active transistor properties with DS-LOCOS process. Open marks in the figure are the case of 170% spacer overetching, and filled marks are 230%. For the isolation etching, sp1 to sp6 in the figure are the case of 50% overetching, and sp7 is 100%. Channel stop implantation dose were split into 1.0×10^{13} atoms/cm^2 for sp1 and sp4, 1.2×10^{13} atoms/cm^2 for sp2 and sp5, and 1.4×10^{13} atoms/cm^2 for sp3 and sp6. The channel stop implantation energy was fixed to 120 keV of ^{11}B. The results showed that active transistor parameters also were critically affected by the spacer overetching percent rather than channel stop implantation conditions. $G_{m,max}$ and V_t plots in terms of channel width variation showed two distinct groups according to spacer overetching percent. Lower overetching percent in spacer etching produced nearly no loss in effective channel width and less V_t deviation showing slight inverse narrow width effect. In the case of higher overetching in spacer etching, $2\Delta W$ was about 0.1 μm, which was well coincident with the bird's beak length shown in Fig. 2(b). This large bird's beak is the main cause of significant V_t deviation below 0.25 μm channel width, showing conventional-style narrow width effect. For source/drain junction, however, higher overetching percent in spacer etching showed better junction characteristics such as lower junction leakage and higher junction breakdown voltage as shown in Fig. 4. Therefore, there is a trade-off in optimization between transistor parameters and junction properties.

Figure 5 shows isolation ability of DS-LOCOS at narrow isolation spacing. For this experiment, both dose and energy of channel stop implantation were split, and MTO thickness was varied from 200 to 300 Å. Punchthrough voltages between n^+ regions were monitored with the substrate bias of -1 V. As a result, no punchthrough voltage degradation with the reduction of isolation spacing down to 0.20 μm was found for all implantation conditions we tried. The differences of monitored punchthrough voltages between split conditions were considered to be caused by different junction breakdown voltages because in our experiment conditions junction breakdown always occurred earlier than real punchthrough between adjacent n^+ regions.

IV. CONCLUSION

Double spacer LOCOS process with shallow recess of silicon (DS-LOCOS) has been developed. The process does not have intentional silicon etching step but achieves the shallow recess of silicon through nitride overetchings. The experimental results show that 100 Å-thick spacer nitride is enough for the suppression of the bird's beak encroachment when MTO spacer thickness is over 200 Å. Also, the DS-LOCOS achieves over 80% of field oxide volume ratio, superior planar surface, bird's beak length of 0.03 μm/side, and no degradation in punchthrough voltage down to 0.20 μm isolation spacing. Thus the DS-LOCO is a simple and very productive isolation technology suitable for 0.20 μm design rule.

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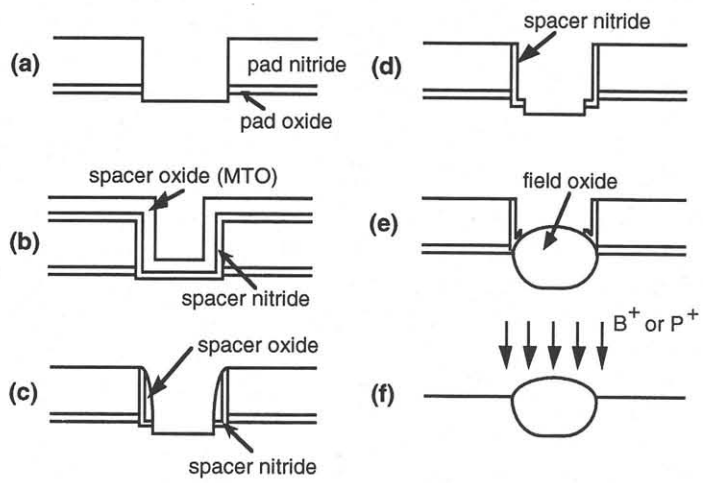

Fig. 1. A process sequence of the DS-LOCOS : (a) formation of conventional LOCOS structure with overetching in isolation etching; (b) deposition of spacer nitride and spacer oxide; (c) spacer formation with overetching; (d) spacer oxide removal; (e) field oxidation; and (e) channel stop implantation through field oxide.

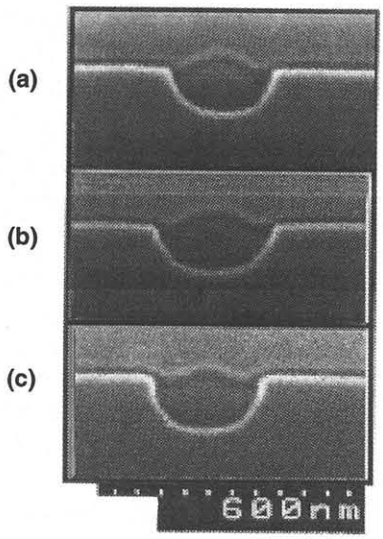

Fig. 2. Field oxide profile after gate cleaning.
Overetching in isolation etching : (a), (b) : 50 %, (c) : 100 %,
overetching in spacer etching : (a), (c) : 170 %, (b) : 230 %

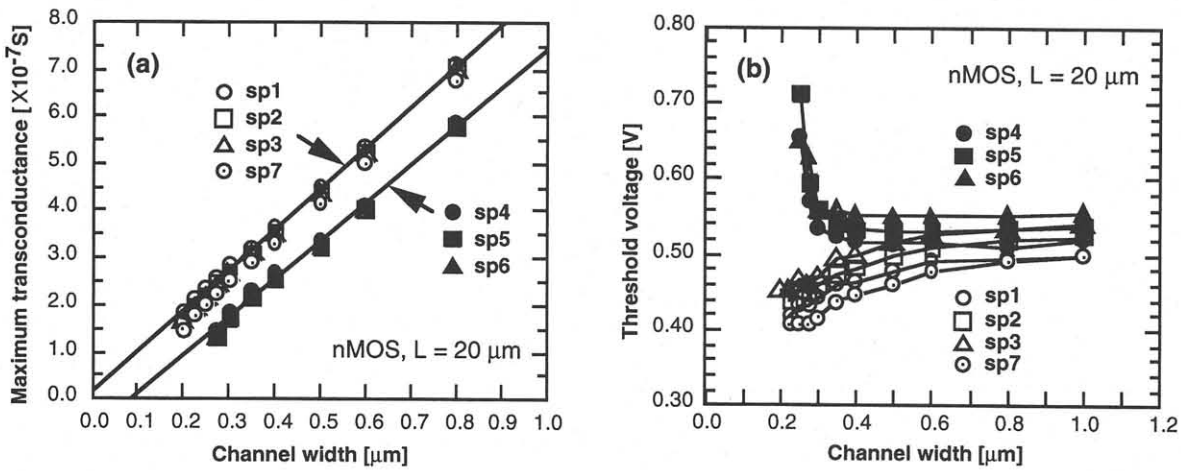

Fig. 3. (a) Gm,max vs. channel width; (b) Vt vs. channel width. Open marks are the case of 170 % spacer overetching, and filled marks are 230 %. sp1 to sp6 are the case of 50 % overetching in isolation etching, and sp7 is 100 %. Channel stop implantation dose were split into; sp1 & sp4 : $1.0X10^{13}$ atoms/cm^2, sp 2, sp 5, & sp 7 : $1.2X10^{13}$ atoms/cm^2, sp 3 & sp 6 : $1.4X10^{13}$ atoms/cm^2. Implantation energy was fixed to 120 keV of B^{11}.

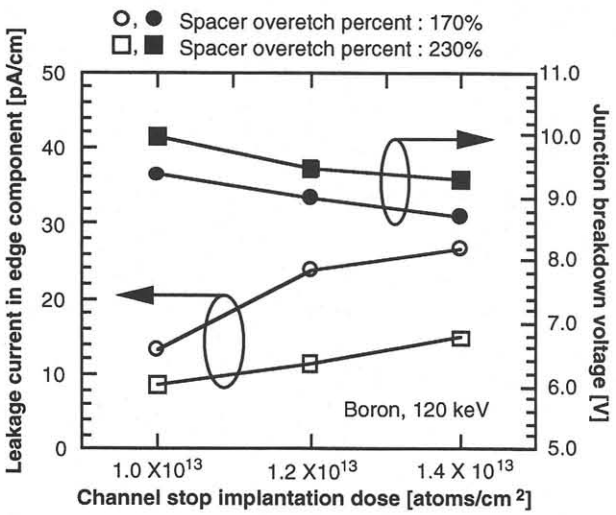

Fig. 4. Junction leakage current and breakdown voltage as a function of channel stop implantation dose with variation of spacer overetch percent.

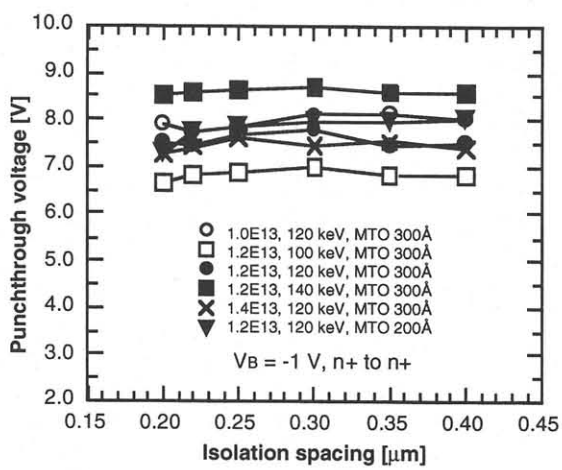

Fig. 5. Punchthrough voltage vs. isolation spacing with various channel stop boron implantation conditions and MTO thicknesses.