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CMP with Pad-Press Ring for Superior Uniformity Performance

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We have studied a CMP system with a ring-shaped pressure plate, called Pad-Press Ring (PPR), to control the pad-profile during polishing. PPR works as an excellent *in-situ* pad-profile controller and improves the polishing uniformity drastically. This system does not need the complicated *ex-situ* pad-profile control, using the conventional film-backed carrier, two-layered pad, and fumed silica slurry. The non-uniformity of 6 % calculated by (Max − Min) ÷ (2 × Average) is obtained with a wafer-edge exclusion length of 5 mm.

Introduction

Recently CMP (Chemical Mechanical Polishing) has become one of the most important technology for global planarization in ULSI multi-level interconnection[1]. It is a main issue in CMP to improve the polishing uniformity which causes the thickness variation of interlayer dielectrics[2][3]. The polishing non-uniformity is mainly attributed to the non-uniform distribution of polishing pad surface. Therefore a strict control of pad surface profile is required to improve the polishing uniformity. The pad-profile is usually controlled with a diamond dress-tool between wafer polishing. But a great deal of experience is necessary to control the pad-profile. To solve these issues, we've already proposed a new CMP system with a ring-shaped pressure plate, called Pad-Press Ring (PPR), to control the pad-profile during polishing[4]. In this paper, we describe the availability of the PPR as an *in-situ* pad-profile controller.

In-situ Pad-Profile Control

Fig. 1 shows the CMP system used in the present study. A ring-shaped pressure plate, called Pad-Press Ring (PPR), presses the polishing pad on the platen with an independent pressure P_p during wafer polishing. As shown in Fig. 2, the center of PPR is located on the same radius R_w of the platen as wafer-center located. The PPR has an inner and outer radius of r_{p1} and r_{p2}, respectively. The inner-radius r_{p1} is same (or larger) as that of wafer r_W. The PPR is made of resin and its surface is almost flat. The intervals being pressed by PPR and wafer depend on the radius R on the platen.

Fig. 3 compares the *in-situ* pad-profile images between conventional CMP (a) and CMP with the PPR (b). The pad surface under the near wafer-center is pressed by the wafer for longer time than that under the near wafer-edge in conventional CMP. As deformation of the pad surface depends on time pressed by the wafer, the pad-profile becomes undesirable U-shaped hollow. The undesirable pad-profile is corrected as flat as possible by the reasonable PPR pressure.

Here the variation of the pad deformation is estimated roughly by the following suppositions, the value of pad deformation is proportional to the pressure and pressing time, and wafer pressure and PPR pressure are always constant and uniformed at each whole surface.

Fig. 4 shows the distributions of the pad deformation. As the value of pad deformation at the near wafer-center is maximum and at the wafer-edge is minimum in the conventional CMP [wafer only : curve (a)], the polishing rate at the near wafer-edge is supposed to be higher than that at the near wafer-center even if the wafer is rotated. On the other hand, the pad deformation profile is reformed to almost straight line at the wafer region, as shown by curve (c), when the PPR pressure P_P is optimized. It is expected that the polishing rate in the system with PPR should be uniformed from wafer-center to wafer-edge, because the polishing rate variation caused by the pad-deformation can be balanced by the wafer rotation.

Experimental

The TEOS-based PECVD (P-TEOS) oxide deposited on silicon wafers were polished with conventional fumed-silica slurry adjusted by KOH to demonstrate the PPR, where $r_W = 75$ mm (6 inch wafer), $r_{P1} = r_W = R_W$, $r_{P2} = 1.4\ R_W$, $P_W = 0.5$ kg/cm^2, platen rotation speed = 60 rpm, carrier rotation speed = 10 rpm, slurry flow rate = 150 cc/min, respectively. A conventional film-backed carrier (utilizing a backing film) and two-layered (soft / hard) pad were used for this demonstration. Stock removal thickness of P-TEOS oxide was about 800 nm through this work. It should be remarkable that the pad surface before polishing was almost flat.

Results and Discussion

Polishing rate across the wafer diameter obtained for various ratio of PPR pressure to the wafer pressure (P_P/P_W) values are shown in Fig. 5. From this figure, the uniformity in polishing rate for the conventional CMP ($P_P/P_W = 0$) is quite poor, especially near the wafer-edge. The polishing rate profile is gradually corrected and becomes to almost flat as the P_P/P_W value is increased. These results are good agreements with the before-described argument, suggesting that the pad-profile is well controlled by the PPR. The PPR works as an excellent pad-profile controller and the embarrassing *ex-situ* pad-profile control with a diamond dress-tool, which is usually optimized by the great deal of cut-and-try, is led to unnecessary.

The dependence of non-uniformity on P_P/P_W for various edge exclusions is shown in Fig. 6. The non-uniformity is improved from 30 % to 6 % in calculation of (Max − Min) ÷ (2 × Average) for a wafer-edge exclusion length of 5 mm, when the P_P/P_W value is increased from 0 to 1.6. These results suggest that the *in-situ* pad-profile control with the PPR is very effective in improving the polishing uniformity.

Conclusion

PPR works as an excellent *in-situ* pad-profile controller instead of a complicated *ex-situ* pad-profile control with a diamond dress-tool. The CMP system with PPR has a great capability for improving the polishing uniformity.

Acknowledgment

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Reference

[1] M. A. Martines, Solid State Technology, Vol. 37-5, p. 26-31, May 1994

[2] K. Achuthan, Proceeding of CMP-MIC, p. 32-39, Feb. 1996

[3] P. W. Freeman, Proceeding of CMP-MIC, p. 57-60, Feb. 1996

[4] T. Murakami, Proceeding of VMIC, June 1996

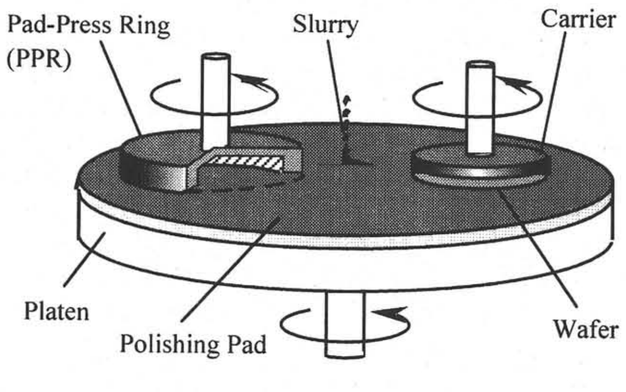

Fig. 1 The Schematics of CMP system with PPR.

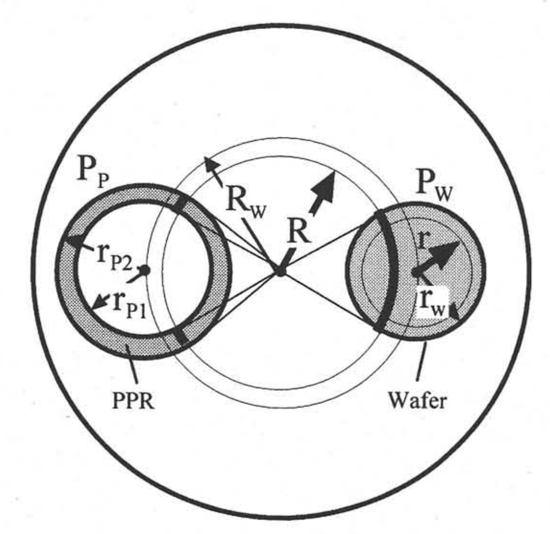

Fig. 2 Definition of parameters used in text.

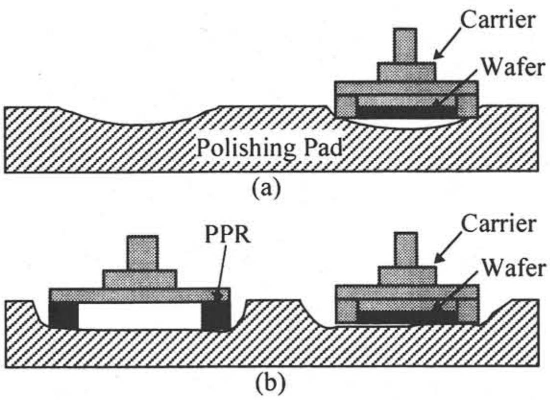

Fig. 3 The pad profile image during polishing without PPR (a) and with PPR (b).

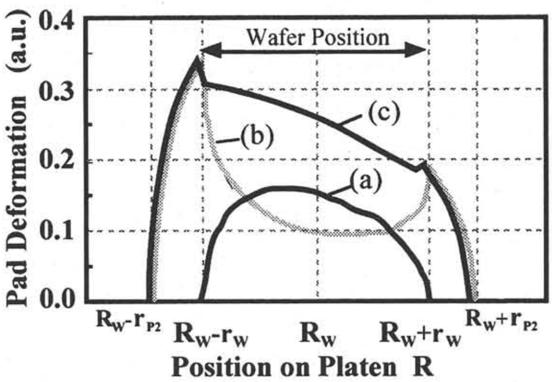

Fig. 4 The distribution of pad deformation, by wafer (a), by PPR (b), and by wafer and PPR (c).

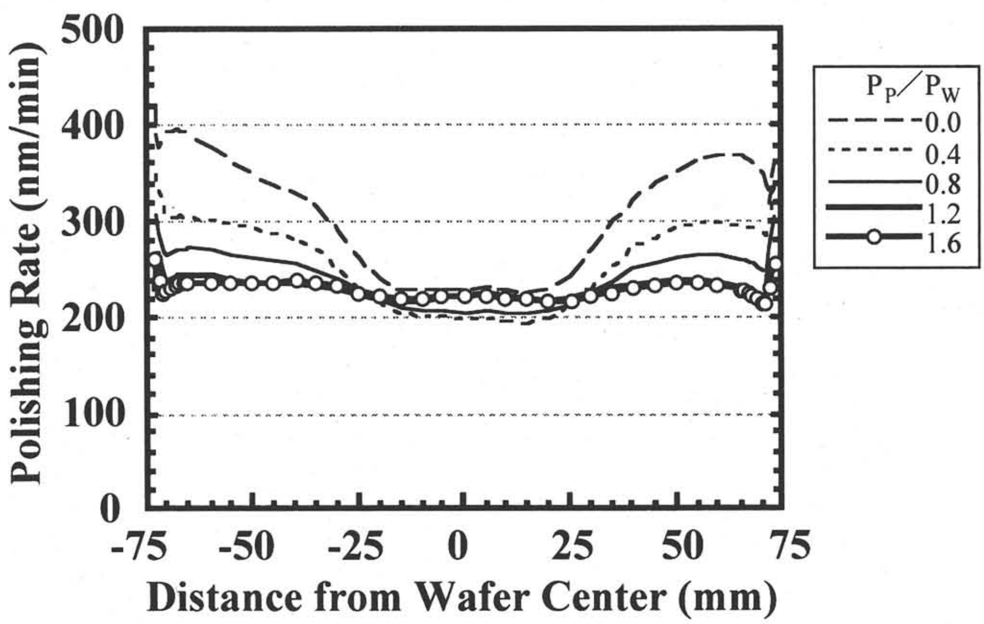

Fig.5 Polishing rate obtained for various P_P/P_W values.

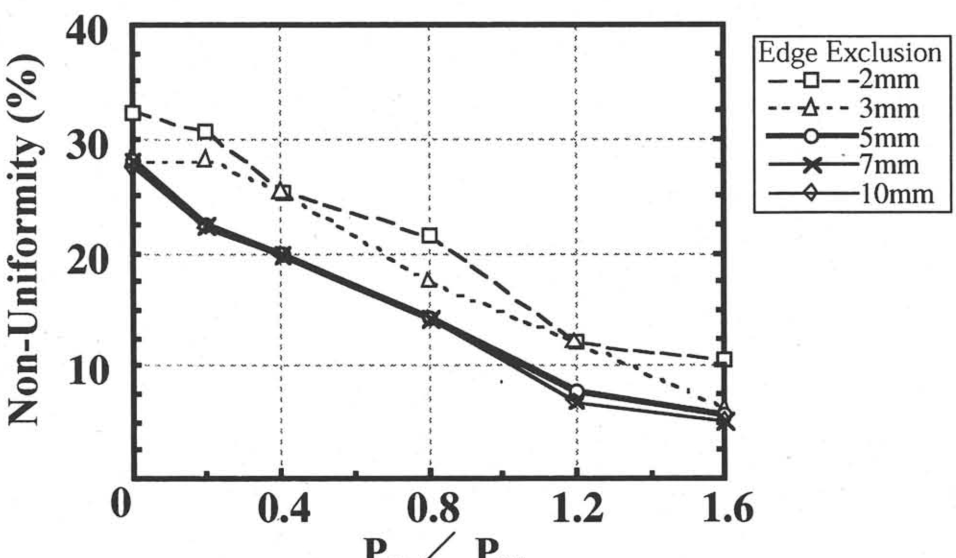

Fig. 6 The non-uniformity of the polishing rate according to the P_P/P_W values.