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Polysilicon Encapsulated LOCOS for Deep Submicron CMOS Lateral Isolation

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ABSTRACT

In this paper it will be shown that polysilicon encapsulated LOCOS (PE-LOCOS) is a feasible candidate as a lateral isolation technique for 0.25μm CMOS technologies. This isolation technique features limited process complexity, excellent bird's beak dimension control, gate oxide integrity and transistor narrow channel behaviour. The influence of recessed field oxide formation on bird's beak dimensions, and isolation-induced stress measurements will be presented and discussed.

1. INTRODUCTION

Local oxidation of silicon (LOCOS) is, together with other variants like Poly Buffered LOCOS (PBL), the most widely used technique for achieving lateral isolation in CMOS processing. Unfortunately, the lateral encroachment of the field oxide under the nitride mask and the nitride mask lifting, which occur for small active area regions, are usually the limiting factors for the scaling of those techniques to 0.25μm CMOS or smaller generations[1]. Polysilicon Encapsulated LOCOS[2], an isolation technique based on standard LOCOS, and which introduces limited processing complexity, has been proposed as a viable sub-micrometer isolation technology[3].

2. PROCESS DESCRIPTION

The process sequence used is shown schematically in fig. 1. A stack consisting of 15nm thermal oxide and 200nm LPCVD nitride is photolithographically patterned and subsequently etched. After resist strip, an HF solution is used to undercut the nitride and create a 50nm-deep cavity into the pad oxide. The exposed silicon surfaces are then re-oxidised and a 20nm-thick amorphous silicon (α-Si) layer is deposited in order to fill the cavity. This silicon-filled cavity retards the diffusion of oxidising species during field oxidation and limits the formation of the bird's beak. After field oxide growth and removal of the nitride/pad oxide stack, processing continues following a standard, twin well CMOS with 6nm gate oxide process flow.

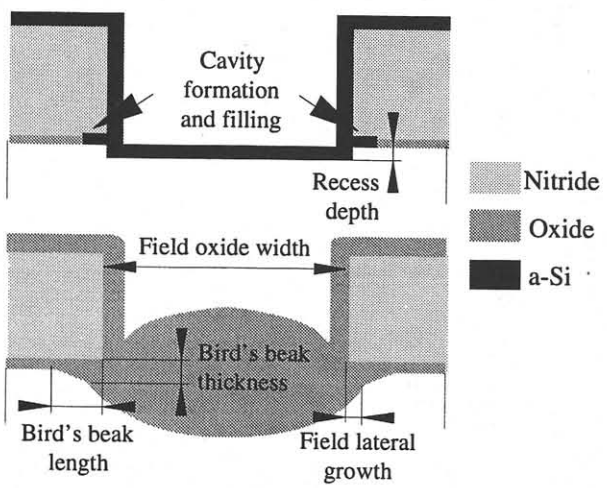

Figure 1: Polysilicon encapsulated LOCOS fabrication process sequence, including definition of dimensions.

3. RESULTS AND DISCUSSION

It has been found that cavity dimensions can be controlled in a reproducible way, independent of feature density and shape, and thus do not pose a manufacturability problem. Besides that, the filling of the cavities with amorphous silicon could be successfully performed for a wide range of cavity depths and pad oxide thicknesses.

The influence of the cavity and the recess depth into the silicon (as shown in fig. 1, top) on bird's beak formation have been evaluated by cross-sectional SEM. For this study, a matrix of experiments was defined with the following parameters: presence or absence of a cavity into the pad oxide (all samples were encapsulated with a 20nm-thick amorphous silicon layer), and recess depth into the silicon after dry etch of the nitride/pad oxide stack, ranging from 20 to 180nm.

In fig. 2 bird's beak thickness is plotted vs. recess depth. The significant decrease of bird's beak thickness which is obtained on the samples with cavity in comparison with the samples which have no cavity (but only amorphous silicon encapsulation), confirms that the silicon filled cavity plays a key role in limiting the formation of the bird's beak. On the other hand, it can also be observed that a larger recess into the silicon results in a clear increase of bird's beak dimensions. This is a consequence of the increase of silicon area which is exposed during field oxidation. Therefore, it can be concluded that recessed field oxides can only be created at the expense of losing bird's beak dimension control, and therefore compromise deep submicron compatibility. However, well controlled bird's beaks are obtained for lim-

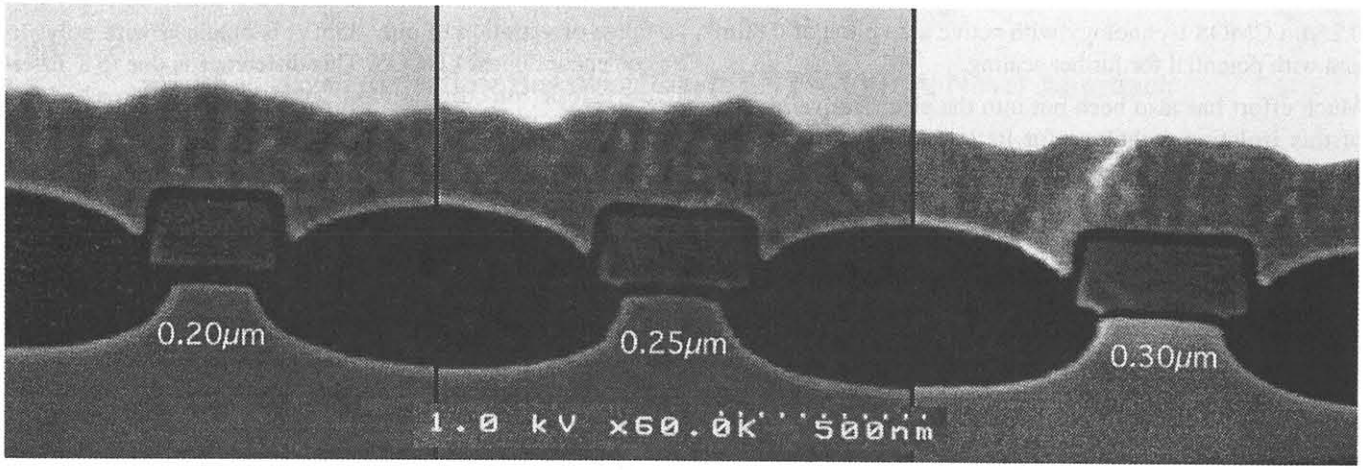

Figure 4: Cross section SEM pictures corresponding to 0.2, 0.25 and 0.3μm-wide isolated active area regions fabricated with polysilicon encapsulated LOCOS

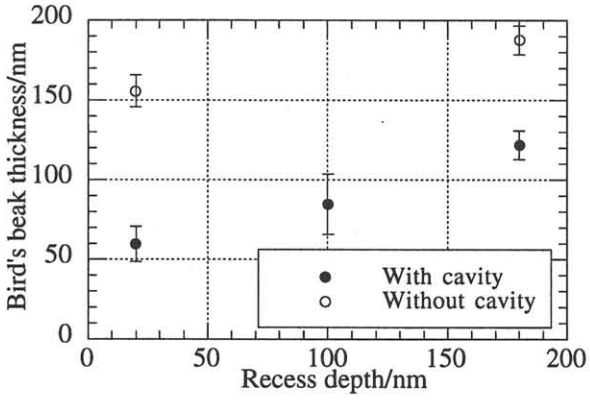

Figure 2: Bird's beak thickness vs. recess depth (all samples had a 20nm α-Si encapsulation)

ited recess.

The field oxide thickness reduction which occurs for small active area spacings has been evaluated for different field oxidation temperatures and thicknesses. Stress effects and 2-dimensional oxidation limitation result in a significant reduction of thickness with decreasing field oxide width. The field oxide thinning obtained for a field oxide grown at 975°C in wet ambient is shown in fig. 3. It is expected that thinning can be significantly reduced by growing the field oxide at higher temperature and/or in a dry ambient[4].

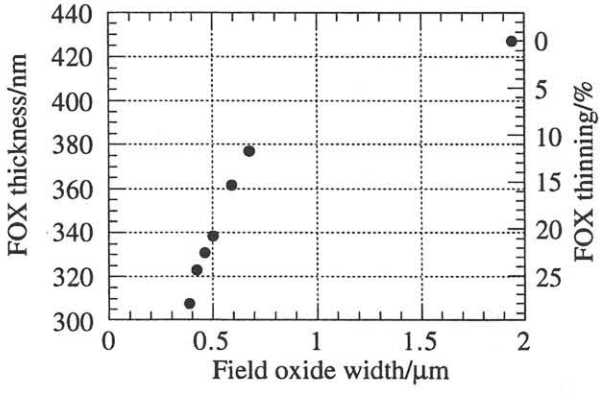

Figure 3: Field oxide thickness as a function of field oxide width corresponding to a wet oxide grown at 975°C

In fig. 4, a series of SEM cross section photographs corresponding to 0.2, 0.25 and 0.3μm isolated active area regions surrounded by wide, 450nm-thick field oxide regions is shown. It should be noted that isolated active areas are the most sensitive to nitride mask lifting, and thus correspond to the worst case condition. Even in these extreme conditions, the maximum oxide thickness under the nitride mask is limited to around 60nm for the 0.2μm active area.

In order to study the isolation-related stress, Raman spectroscopy measurements have been performed on PBL and polysilicon encapsulated LOCOS samples, as shown in fig. 5. A positive Raman shift on the graph indicates compressive stress, whereas a negative shift indicates tensile stress. The position of the active area regions is indicated in the figure by black stripes. The tensile stress at the bird's beak-tip (marked with a grey circle on the figure) which can be observed for the PBL samples, and which is known to be a possible cause of defect formation in the substrate[5], could not be observed on the polysilicon encapsulated LOCOS samples. On the other hand, the higher compressive stress in the active area of polysilicon encapsulated LOCOS is not expected to enhance defect creation.

All results presented so far show that, from the structural point of view, polysilicon encapsulated LOCOS is an isolation technique which is suitable for implementation in a

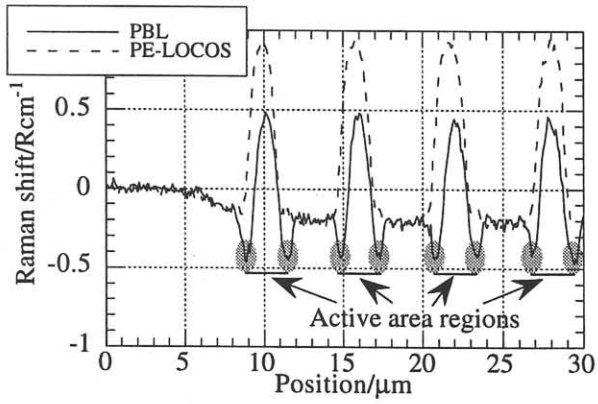

Figure 5: Raman shift as measured on PBL and polysilicon encapsulated LOCOS samples. Notice the absence of tensile stress at the bird's beak for PE-LOCOS

0.25μm CMOS technology with active area pitch of 0.8μm and with potential for further scaling.

Much effort has also been put into the electrical validation of this isolation technique for its integration in a CMOS process. Gate oxide quality on active area edges, active area dimension control and threshold voltage stability and controllability for narrow width transistors have been evaluated.

In fig. 6, charge to breakdown distributions are shown as measured on large area and perimeter intensive, field overlapping gate oxide capacitors. The comparison between rectangular capacitors with 0.58mm^2 surface and 4000μm perimeter, and two kinds of perimeter intensive capacitors with active area strip widths of 0.4 and 2.0μm, respectively, and a perimeter of 10cm, clearly shows that no perimeter related gate oxide integrity degradation could be observed. This result was confirmed by emission microscopy measurements, which showed that breakdown was not occurring at the active area edges.

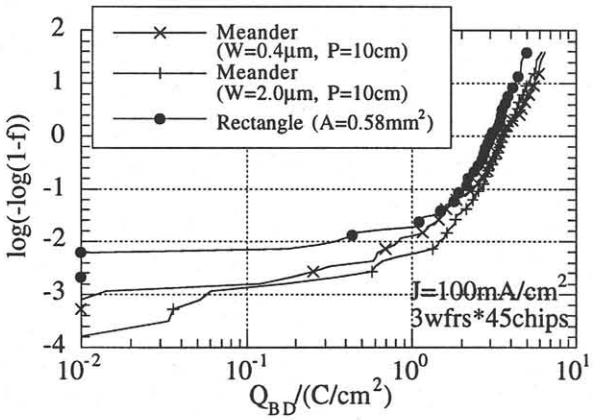

Figure 6: Charge to breakdown distribution for different overlapping gate oxide capacitors

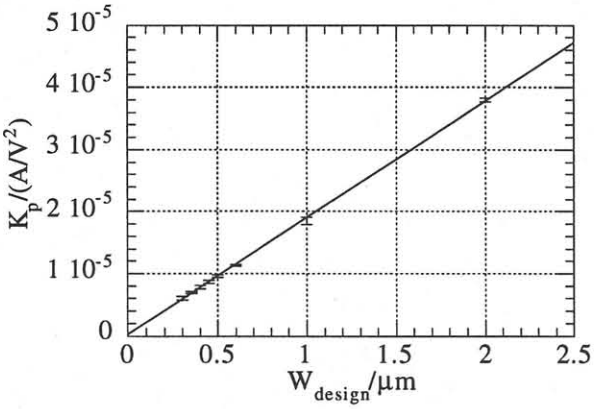

Figure 7: Maximum transconductance K_p vs. NMOS transistor design width

Figure 7 shows the maximum transconductance (Kp) measured on NMOS transistors as a function of their design width (an oversize of 50nm per side was applied during mask making). Excellent linearity can be observed down to the minimum dimensions that could be defined using DUV lithography. Threshold voltage variation vs. transistor width is shown in fig. 8, together with the results obtained with a PBL isolation scheme that was used as a reference. A different threshold voltage roll-off behaviour, with a total range of variation of only 35mV, is obtained with polysilicon encapsulated LOCOS. This difference is due to a different slope on the silicon at the active area edges. Comparable results were obtained for the PMOS transistors.

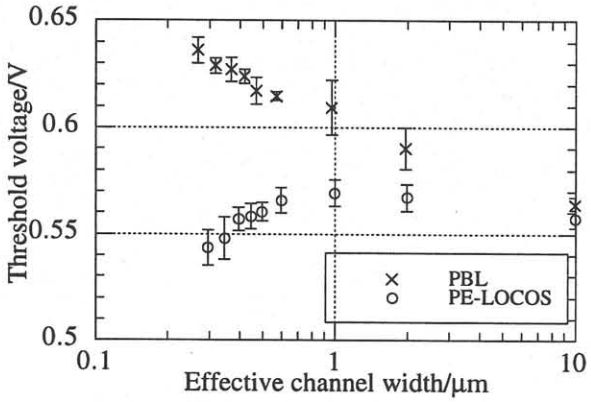

Figure 8: NMOS threshold voltage vs. effective channel width

4. CONCLUSIONS

It has been shown that polysilicon encapsulated LOCOS is a lateral isolation technique with very limited process complexity which can be used for 0.25μm CMOS with active area pitch of 0.8μm or smaller.

Excellent bird's beak dimension control has been demonstrated on active area regions as small as 0.2μm. Tensile stress at the bird's beak edge is much reduced as compared to a PBL reference. Very good results concerning gate oxide integrity and narrow channel effects have been presented.

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