Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 52-54

Invited

Deposition and Characterization of Silicon-Germanium Alloy Thin Films on Oxide

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Polycrystalline silicon-germanium ($Si_{1-x}Ge_x$) alloy films are a novel class of electronic materials for use in thin-film transistors (TFTs) and other thin film applications. This paper summarizes the development of a deposition technology for $Si_{1-x}Ge_x$ alloy thin films on oxide and the structural and electrical properties of the resulting polycrystalline $Si_{1-x}Ge_x$ films.

$Si_{1-x}Ge_x$ alloy thin films have been formed on oxide-coated Si substrates by Plasma-Enhanced Very-Low-Pressure Chemical Vapor Deposition (PE-VLPCVD). The deposition of polycrystalline films by the pyrolysis of SiH_4 and GeH_4 gases at temperatures $\leq$600°C has been accomplished by two methods: thermal growth on a thin Si buffer layer (VLPCVD) and plasma-enhanced deposition on oxide (PE-VLPCVD). In both cases, the incorporation of Ge into the polycrystalline film increases rapidly with gas ratio of $GeH_4/(SiH_4+GeH_4)$, and $Si_{1-x}Ge_x$ growth rates as well as grain sizes increase with Ge content. Furthermore, for both modes of deposition, the transition temperature between polycrystalline and amorphous deposition is lower for $Si_{1-x}Ge_x$ than Si, an effect consistent with the lower melting point of Ge compared to Si. On the other hand, compared to thermal growth, plasma-enhanced deposition of poly-$Si_{1-x}Ge_x$ leads to smaller grain sizes but benefits from the effects of plasma in promoting higher growth rates and decreased amounts of carbon and oxygen contamination in the films. Plasma-enhanced deposition also results in direct deposition of poly-$Si_{1-x}Ge_x$ onto oxide as well as improved structural film properties such as smoother surface morphology and a more columnar, {220}-dominant grain texture.

To address the decreased grain sizes in plasma-deposited poly-$Si_{1-x}Ge_x$ films, two post-deposition processing techniques were explored: low-temperature plasma deposition of amorphous $Si_{1-x}Ge_x$ with subsequent crystallization, and amorphization of poly-$Si_{1-x}Ge_x$ by Si^+ implantation with subsequent recrystallization. Deposition by PE-VLPCVD of amorphous $Si_{1-x}Ge_x$ followed by a crystallization anneal in N_2 at 600°C forms poly-$Si_{1-x}Ge_x$ films having even smoother surface morphologies compared to plasma-deposited poly-$Si_{1-x}Ge_x$ films, with grain sizes enlarged by an order of magnitude and a weak {111} grain texture typical of thermally grown poly-Si films. Hydrogen that is incorporated during plasma deposition of amorphous $Si_{1-x}Ge_x$ films at 400°C

evolves completely during the crystallization process without disrupting the smooth surface morphology. Crystallization of plasma-deposited amorphous $Si_{1-x}Ge_x$ films occurs faster for films with higher Ge contents. Similarly, the converse process of amorphization by Si^+ implantation occurs at lower doses for poly-$Si_{1-x}Ge_x$ films than for poly-Si. Recrystallization of Si^+ implant-amorphized poly-$Si_{1-x}Ge_x$ films at 600°C results in a modified polycrystalline $Si_{1-x}Ge_x$ film with surface morphologies not quite as smooth as amorphous-crystallized films but with the largest observed grain sizes, up to 1.3μm in 25% Ge films of 1000Å thickness.

The effects of Ge on the electrical properties of dopant-implanted poly-$Si_{1-x}Ge_x$ films were also studied. Van der Pauw structures were fabricated using structurally optimized poly-$Si_{1-x}Ge_x$ films with a maximum process temperature of 600°C. Hall effect measurements of heavily doped poly-$Si_{1-x}Ge_x$ films with $x \leq 20\%$ suggest that Ge enhances phosphorus segregation at grain boundaries whereas it enhances the activation of carriers from boron dopants. Hall mobilities in both n-type and p-type poly-$Si_{1-x}Ge_x$ films increase as functions of Ge content; the Hall mobility in an n-type poly-$Si_{0.80}Ge_{0.20}$ film is 50 cm^2/V-sec. Results from temperature-dependent resistivity measurements of doped poly-$Si_{1-x}Ge_x$ films ($x \leq 0.20$) indicate that conduction occurs by thermionic emission of free carriers over potential barriers at grain boundaries. For n-type films, poly-$Si_{1-x}Ge_x$ resistivities are comparable to that of poly-Si, with similar grain boundary barrier heights; p-type poly-$Si_{1-x}Ge_x$ films, on the other hand, have lower resistivities than p-type poly-Si with potential barrier heights that decrease dramatically with Ge content. At lower dopant concentrations, the improvements in poly-$Si_{1-x}Ge_x$ resistivities become more pronounced; at higher dopant concentrations, conduction becomes limited by scattering within the grains.

Top-gate self-aligned poly-$Si_{0.82}Ge_{0.18}$ thin-film transistor devices (TFTs) were fabricated with a maximum process temperature of 620°C. Prior to hydrogenation, n-MOS and p-MOS poly-$Si_{1-x}Ge_x$ TFTs exhibit poorer device characteristics compared to poly-Si control TFTs in terms of on/off current ratios, threshold voltages, subthreshold slopes, and leakage currents. One promising feature of the $Si_{1-x}Ge_x$ devices, however, is that the p-MOS field-effect mobility is greater than the corresponding n-MOS mobility by almost an order of magnitude, consistent with the decreased potential barrier heights at grain boundaries observed in p-type compared to n-type poly-$Si_{1-x}Ge_x$ films. The process of plasma hydrogenation is effective at improving device characteristics, with $Si_{1-x}Ge_x$ TFTs responding just as well if not better to hydrogenation compared to Si TFTs. Passivation rates are similar for Si and $Si_{1-x}Ge_x$ TFTs in that the threshold voltages and subthreshold slopes have a faster response to hydrogenation compared to field-effect mobilities. Although device properties improve quite

dramatically, estimated grain boundary trap state densities extracted from transfer characteristics remain higher in $Si_{1-x}Ge_x$ than in Si and may be attributed to a high density of Ge dangling bonds at the gate dielectric interface. Once this interface is improved, the potential of poly-$Si_{1-x}Ge_x$ alloy materials can be better utilized for higher performance low-temperature-processed devices.

High-temperature processed poly-Si-capped poly-$Si_{0.9}Ge_{0.1}$ TFTs with thermal oxide were found to have the a mobility of 51 cm^2/V-sec for p-channel devices and 41 cm^2/V-sec for n-channel devices. This is compared to the hole mobility of 27 cm^2/V-sec and the electron mobility of 45 cm^2/V-sec for similarly processed poly-Si TFTs. Low-temperature processed poly-$Si_{0.88}Ge_{0.12}$ TFTs were also measured to have mobility of 35 cm^2/V-sec for holes and 28 cm^2/V-sec for electrons. This is compared to a hole mobility of 26 cm^2/V-sec and electron mobility of 29 cm^2/V-sec for similarly processed poly-Si TFTs.

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