Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 527-529

Single Crystalline Silicon Floating Gate Technology for Sub-10 nm Interelectrode Dielectrics

Shigehiko Saida, Yuuichirou Mitani*, Hiroaki Hazama, Shigeru Kammbayashi*, Ichiro Mizushima, Jun-ichi Shiozawa and Yoshio Ozawa

Microelectronics Engineering Laboratory and ULSI Research Laboratories*
Toshiba Corp.

1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi, Kanagawa, 210, Japan
Phone: +81-44-549-2193 Fax: +81-44-549-2248

A novel single crystalline silicon floating gate technology is proposed as the ultimate method to realize defect free memory cells. It is demonstrated that the defect density of interelectrode dielectrics formed on the single crystalline silicon floating gate is at least about one order lower than that formed on the recrystallized polycrystalline silicon floating gate.

1. Introduction

Polycrystalline silicon is widely used as a gate electrode material for LSIs. For flash memory devices, it has been recognized that the crystallinity of floating gate electrodes is a key parameter for improving reliability and/or performance, because the integrity of both interelectrode dielectrics and tunnel dielectrics depends strongly on the electrode crystallinity. For example, leakage currents through interelectrode dielectrics have been shown to decrease by using in-situ phosphorus doped amorphous silicon process instead of phosphorus implanted polycrystalline silicon process for floating gate formation [1]. It has also been shown that the floating gate polycrystalline silicon grain size dominates flash memory erase characteristics [2]. Recently, it has been reported that the amorphous silicon deposition process for floating gate formation has a benefit of improving the retention characteristics [3].

In this paper, on the basis of an interelectrode dielectrics defect generation model, we propose single crystalline silicon floating gate technology to realize defect free memory cells. It is clarified that the single crystalline silicon floating gate technology essentially solves interelectrode dielectrics defect formation. The technology proposed in this work is found to be promising for flash memory devices with sub-10 nm interelectrode dielectrics.

2. Experiment

NAND EEPROM cell array test circuits fabricated with 0.7 μm design rule were used for measuring dielectric defect density and evaluating device reliability. The schematic cross-sectional view of the cell array is shown in Fig. 1 and the lower part of Fig. 5. The cell array consist of 8 memory cells (cell 1- cell 8) and 2 select transistors connected in series between a source and a bitline contact. The memory cell nearest from the source area is named "cell 1" in this text.

Two different process procedures were used to fabricate the floating gates of the test circuits. One was a novel procedure utilizing the lateral solid phase epitaxial method to prepare the single crystalline silicon electrode. As shown in Fig. 2, the amorphous silicon layer deposited on a gate oxide was doped by phosphorus ion-implantation and then crystallized from the seed region formed in the source pattern area. Therefore, the cell 1 is the nearest from the seed region. Another was a conventional procedure to prepare the polycrystalline silicon electrode. In this procedure, the polycrystalline silicon layer was deposited by the LPCVD method and then doped by $POCl_3$ diffusion.

The defect density of interelectrode dielectrics was deduced from the I-V characteristics of the cell array test circuits in the following way. First, theoretical leakage currents through the tunnel dielectrics were calculated on an assumption that the control gates and floating gate of a single cell were electrically shorted. Next, leakage currents between common control gates and substrate were measured, as shown in Fig. 1. Then, the number of interelectrode dielectric broken-down cells was calculated by dividing the measured currents by the theoretical currents. The validity of this method was confirmed with the fact that the measured currents are proportional to the theoretical currents, as shown in Fig. 3.

3. Results and Discussion

By measuring the capacitor structure dependence of interelectrode dielectric breakdown frequency and observing TEM images just at breakdown regions, we identified polycrystalline silicon grain growth during the device fabrication process as the most critical factor in interelectrode dielectric defect generation. According to the generation mechanism, we constructed a novel technology to form single crystalline silicon floating gates as the ultimate method to realize defect free memory cells.

The point of the procedure is that it contains two steps of amorphous silicon layer deposition, as shown in Fig. 2. By adopting this procedure, the contamination level of the tunnel dielectrics from the resist becomes negligible, because the first amorphous silicon layer covers the tunnel dielectrics in the seed patterning step.

Figure 4a shows a cross-sectional TEM image of the memory cell fabricated by the proposed technology. No grain boundary was observed in the floating gate electrode region. It is clearly shown in Fig. 4b that the floating gate electrode was composed of single crystalline silicon with

(100) orientation. (Twin spots were observed in this electron diffraction pattern. One spot of each pair is attributed to the substrate crystal.)

From the above TEM image observation and the electron diffraction pattern measurement, it was confirmed that floating gate electrodes of cells 1 and 2 were composed of single crystalline silicon and those of cells 7 and 8 were composed of recrystallized polycrystalline silicon. Because cells 7 and 8 were about 10 μm away from the seed region, the random nucleation occurred in the amorphous silicon layer at their area before the lateral solid phase epitaxial growth took place.

The leakage current between common control gates and substrate were measured, as shown in Fig. 3. The dielectrics consisted of the ONO structure and its effective thickness was 12 nm. The currents in the cell array fabricated by the conventional procedure were about 2000 times larger than the theoretical currents calculated on the assumption that the control gates and floating gate of a single cell were electrically shorted. The currents in the cell fabricated by the novel procedure were much smaller than the theoretical currents. These results show that the interelectrode dielectrics of 2000 cells were broken down in the conventional cell array and those of no cell were broken down in the novel cell array.

The measured values of interelectrode dielectric defect density are summarized in Fig. 5. It was clearly shown that the defect density depends strongly on the crystallinity of floating gate electrode: note that the defect density of interelectrode dielectrics formed on the single crystalline silicon floating gate electrode (cells 1 and 2) was found to be at least about one order lower than that formed on recrystallized polycrystalline silicon (cells 7 and 8), as expected from the above interelectrode dielectric defect generation model.

In the amorphous silicon recrystallizing process, it is known that silicon films are densified and interface strain is generated. The electrical characteristics of tunnel oxides are reported to depend on the stress generated by the floating gate electrode [4]. Therefore, we investigated whether tunnel dielectric characteristics depend on the floating gate formation method. As shown in Fig. 6, read disturb characteristics has no significant relationship with the crystallinity of the floating gate electrode. This result shows that the single crystalline silicon floating gate process exerts little influence on tunnel oxide reliability.

4. Conclusion

The results obtained in this paper show that the single crystalline silicon floating gate technology essentially solves reliability degradation problems related to defect formation in interelectrode dielectrics. The technology proposed in this work is promising for sub-10 nm interelectrode dielectric films to be used in future flash memory devices.

5. Acknowledgment

We wish to thank M. Koike for evaluating floating gate crystallinity by TEM observation.

6. References

(1)T.Kobayashi, et. al., SSDM '90, P. 191 (1990)
(2)S.Muramatsu, et. al., IEDM '94, P. 847 (1994)
(3)T.Kubota, et. al., IRPS '96, P. 12 (1996)
(4)M.Ushiyama, et. al., IRPS '95, P. 18 (1995)

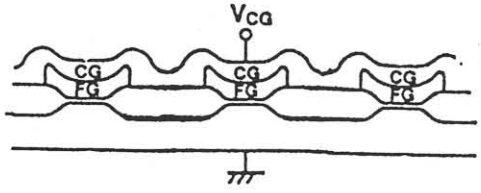

Fig. 1 Schematic cross-sectional view of the EEPROM device used in this work. Leakage currents were measured by applying negative bias (Vcg) to the common control gate electrodes.

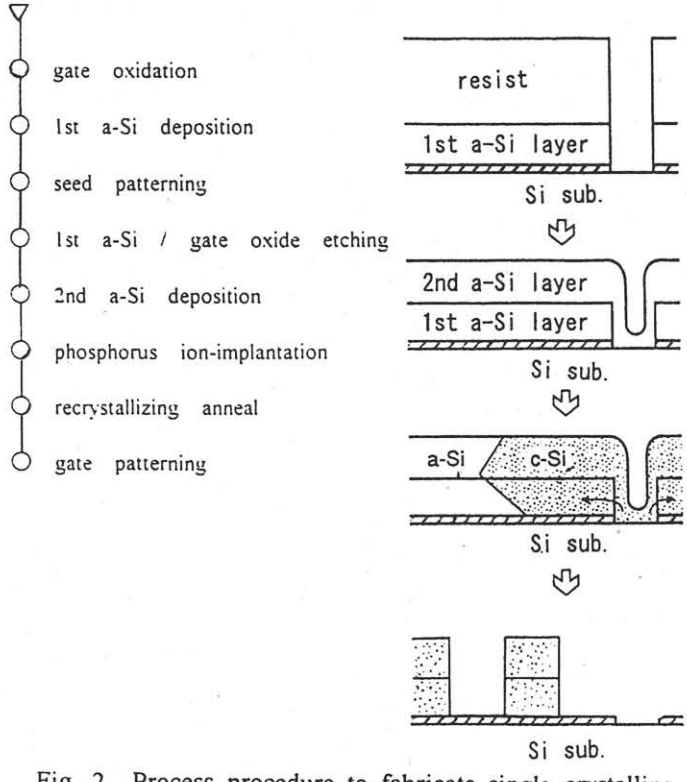

Fig. 2 Process procedure to fabricate single crystalline electrode.

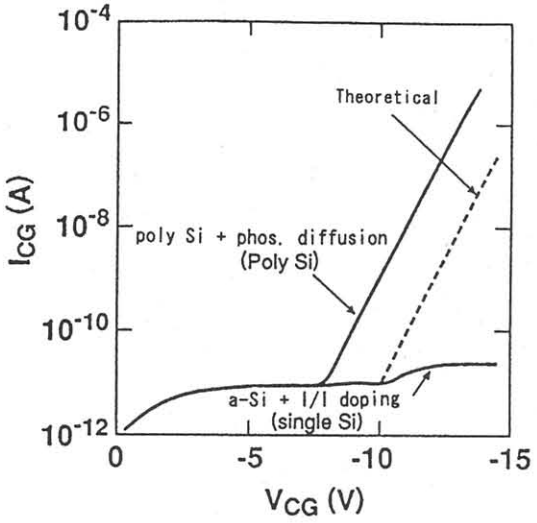

Fig. 3 Example of I-V characteristics between common control gate electrode and substrate. Dashed line shows a theoretical F-N current through tunnel oxide.

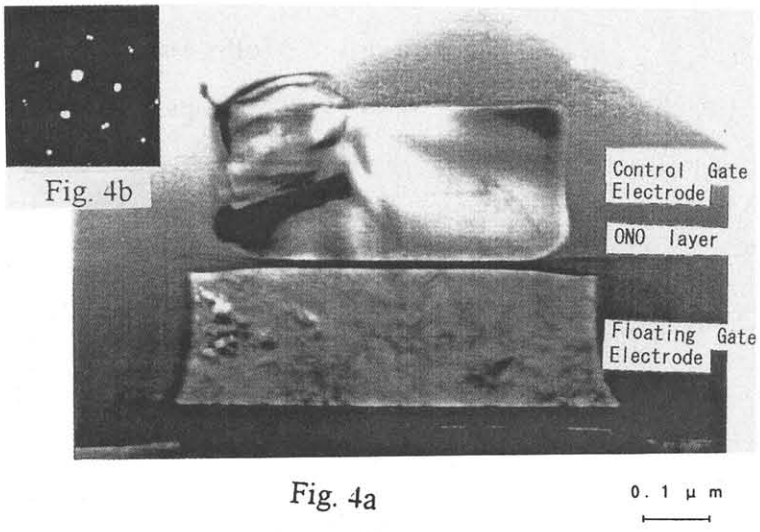

Fig. 4a

Fig. 4 (a) Cross-sectional TEM images of an EEPROM cell fabricated by the single crystalline floating gate process.

(b) Electron diffraction pattern of the floating gate electrode region. One spot of each pair is attributed to substrate crystal.

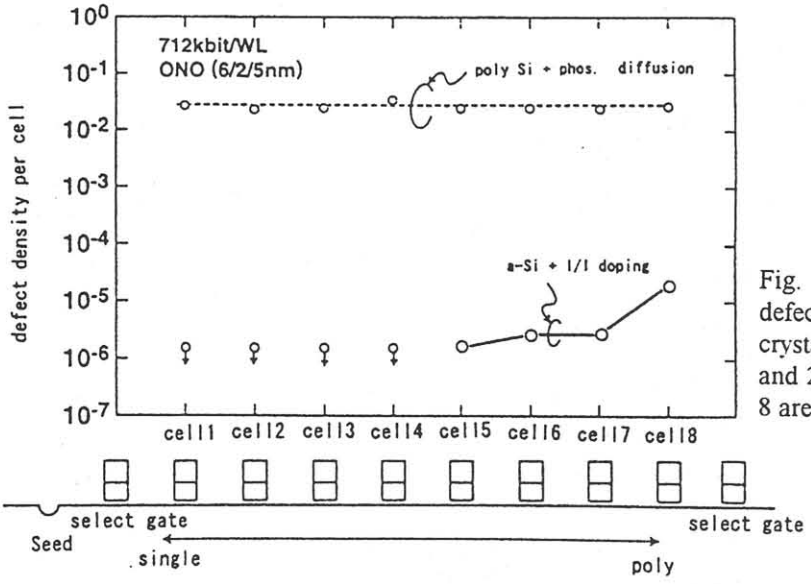

Fig. 5 Dependence of interelectrode dielectric defect density on floating gate electrode crystallinity. Floating gate electrodes of cells 1 and 2 are single crystalline. Those of cells 7 and 8 are polycrystalline.

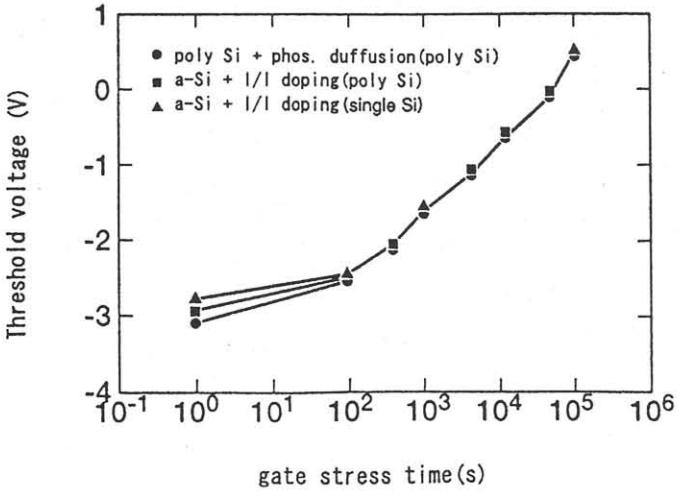

Fig. 6 Dependence of read disturb characteristics on floating gate electrode crystallinity. This characteristics were measured after 10^6 cycles of programming and erasing.