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Reliability of Ultra-Thin Gate Oxides Below 3 nm in the Direct Tunneling Regime

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The reliability of ultra-thin 1.5 nm to 3 nm gate oxide layers during electron injection by direct tunneling is examined in this work. Dielectric breakdown of these ultra-thin SiO_2 layers is defined by the occurrence of complex fluctuations in the direct tunneling current. It is shown for the first time that the time to dielectric breakdown t_{BD} of the ultra-thin gate oxide in the direct tunneling regime is determined by the electrical oxide field strength similar to the case of Fowler-Nordheim tunnel stressing.

1. INTRODUCTION

Recently, operating 0.1 μm MOS transistors with a gate oxide thickness of only 1.5 nm were demonstrated [1]. For these ultra-thin oxide layers direct tunneling of electrons between the poly-Si gate and the Si substrate becomes very important [2-3]. However little is known about the ultra-thin oxide reliability in this case. The time dependent dielectric breakdown (TDDB) during a constant voltage or constant current stress of these ultra-thin gate oxides is defined and examined in the direct tunneling (DT) regime.

2. EXPERIMENTAL

The Si wafers used were 150 mm p/p^+ epi material from Wacker. The wafers received a Piranha treatment followed by an RCA clean. Some wafers were dipped in a 2% HF solution to remove the chemical oxide layer after the SC2 step. The thermal growth of the oxide layers was done in the vertical furnace of an ASM Advance 600 cluster tool. The loading of the wafers was done at 650°C in a 25% O_2/N_2 ambient at a reduced pressure of 1 Torr to limit the growth during this critical step. The temperature ramp-up and a 10 min. stabilisation period was done in 1% O_2/N_2 at atmospheric pressure. This was followed by an oxidation period t_{ox} in 10% O_2/N_2 and cooling in N_2. The electrical evaluation of the gate oxide was done with n^+poly-Si gate MOS capacitor structures. Poly-Si deposition was done in the LPCVD reactor of the cluster tool.

3. RESULTS AND DISCUSSION

The ultra-thin SiO_2 growth characteristics are presented in Fig.1. A linear growth law is observed with an offset at $t_{ox}=0$ due to the growth during the loading, ramp-up and stabilisation step. It is seen from Fig.1 that by reducing the oxidation temperature, the growth of oxide layers as thin as 1.5 nm can still be controlled in a cluster tool. The advantage of the cluster tool over a conventional open furnace lies in the better control of the ambient during the loading of the wafers. The 3 sigma value of the oxide thickness uniformity was 0.04 nm as obtained by ellipsometry. This extremely good oxide thickness uniformity has also been demonstrated from the tunnel current measurements on MOS structures [2-3]. In Fig.2 the exponential increase of the direct tunnel current (DT) in ultra-thin oxide layers below 3 nm is observed with the decrease of the oxide thickness.

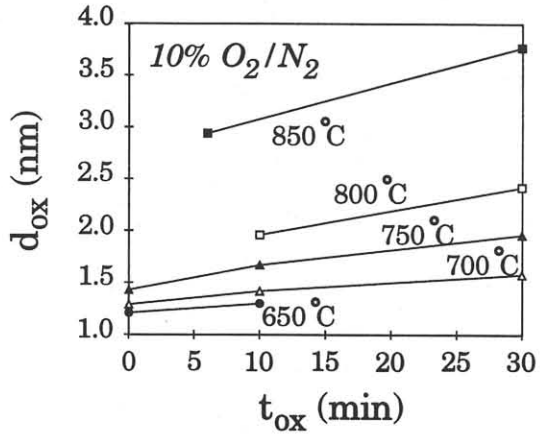

Fig.1 Growth kinetics of ultra-thin SiO_2 layers at 650 to 850°C in 10% O_2/N_2 (SC2 last cleaning).

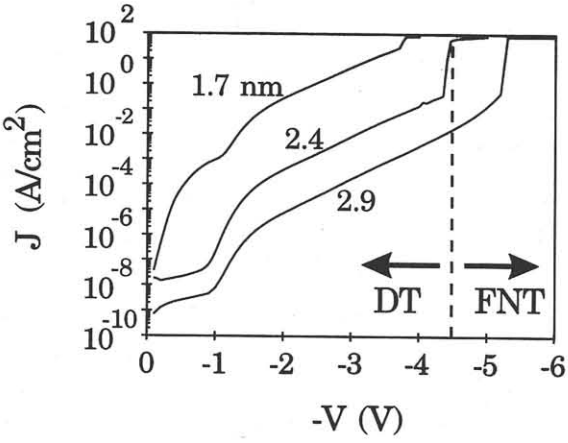

Fig.2 Tunnel current density J in gate oxides below 3 nm (DT: direct tunneling, FNT: Fowler-Nordheim tunneling).

The -4.5 V transition voltage from a FNT to a DT injection mechanism was determined from C-V measurements [4]. The distribution of the gate voltage V corresponding with a 0.01 A/cm^2 direct tunnel current density is compared in Fig.3 for the two different Si wafer cleanings (a: HF last, b: SC2 last). The tail in the distribution is caused by pinholes in the oxide [2]. For both cases a low defect density of 0.3-0.4 defects/cm^2 was measured for these ultra-thin oxides. The difference between the distributions a and b in Fig.3 can be explained by a 0.05 nm smaller oxide thickness in the case of the removal of the chemical oxide prior to oxidation, in good correspondence with the ellipsometric results. In both cases extremely uniform oxide layers were obtained.

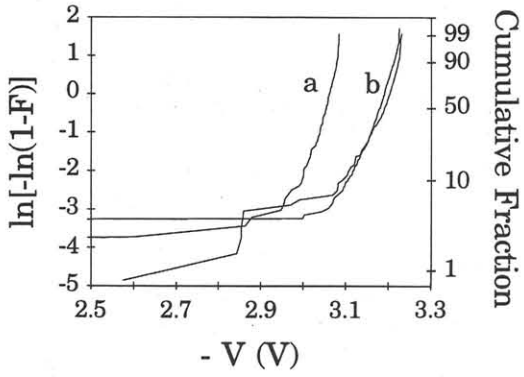

Fig.3 Cumulative distribution of the measured gate voltage V at a 0.01A/cm^2 DT current through a) 2.34nm (HF last) and b) 2.42nm (SC2 last) gate oxide (16 mm^2 area capacitors).

It can be seen from Fig.2 that the gate voltage V at which dielectric breakdown occurs decreases for thinner oxide layers. For the 2.9 nm oxide the breakdown occurs in the FNT regime while for the thinner (2.4 nm and 1.7 nm) gate oxide dielectric breakdown takes place in the DT regime. The oxide reliability was investigated with time dependent dielectric breakdown (TDDB) measurements. In the case of ultra-thin gate oxides below 3 nm soft breakdown occurs [5]. Due to the reduction of the applied power for ultra-thin oxides, the capacitor structure is not destroyed immediately by thermal effects. This is illustrated in Fig.4 and 5 for a 1.7 nm gate oxide.

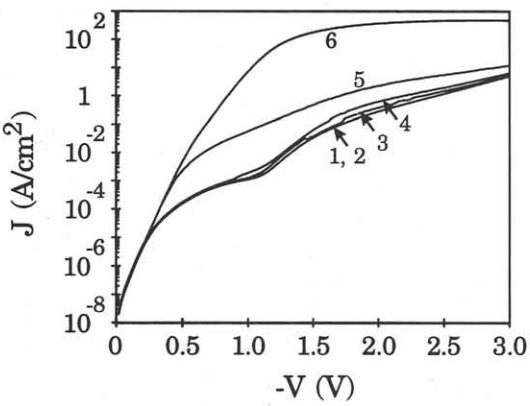

Fig.4 J-V of the 1.7nm gate oxide during the different stages of the oxide wear-out and breakdown. The curves labeled with 1 to 6 correspond with the stress periods indicated in Fig.5.

The gradual wear-out of the ultra-thin 1.7 nm gate oxide during a stress in the DT regime is shown in Fig.4. The evolution of the DT current through this ultra-thin oxide for a constant voltage stress is shown in Fig.5. The small increase of the DT current from time 1 to 2 is explained by the creation of positive charge in the oxide [2,5]. The t_{BD} value is defined as point 2 during the stressing. The occurrence of complex fluctuations in the tunnel current (time 3 and 4) corresponds with the first stage of the ultra-thin oxide dielectric breakdown when a critical number of electron traps is generated locally [7]. A gradual increase of the current is observed (time 4 to 5) before the total dielectric breakdown of the oxide takes place and a direct contact between the poly-Si gate and the Si substrate is created (time 6) due to thermal effects.

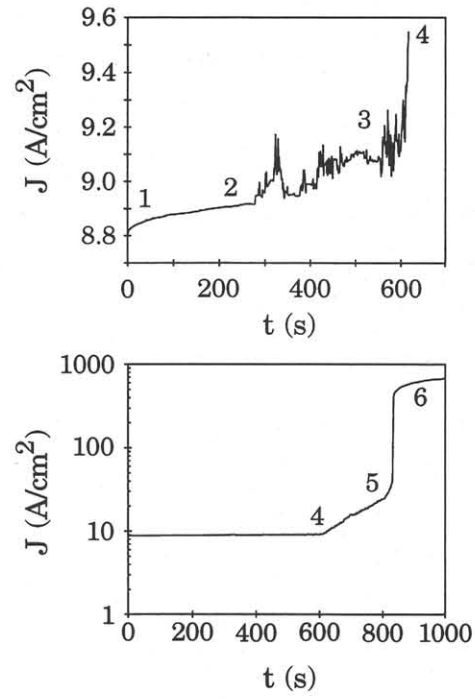

Fig.5 Evolution of the DT current instability in 1.7nm gate oxide for a -3.2 V constant voltage stressing.

The statistical distribution of the intrinsic charge to breakdown Q_{BD} is shown in Fig.6. A model for the intrinsic oxide breakdown has been presented in [7] based on the creation of electron traps and the conduction via traps in the oxide layer. Soft breakdown occurs when a critical number of traps in the oxide is generated; allowing the formation of a conducting path in the oxide between the electrodes (Fig.7). The small Weibull slope of the intrinsic Q_{BD} distribution for thin oxides is predicted by this model [7]. In Fig.8 the good agreement between the experimental and the simulated distribution is demonstrated for the case of a DT stress of a 2.4 nm gate oxide. The Weibull slope is only 1.3. Monte Carlo simulation is used for the electron trap generation assuming a radius of 0.45 nm for the traps [7].

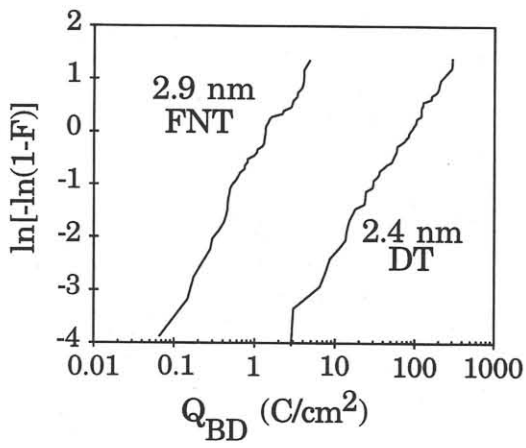

Fig.6 Weibull plot of the Q_{BD} distribution of 2.4 nm and 2.9nm gate oxide for a constant current stress (0.1 A/cm^2 gate injection on 10^{-4}cm^2 capacitors).

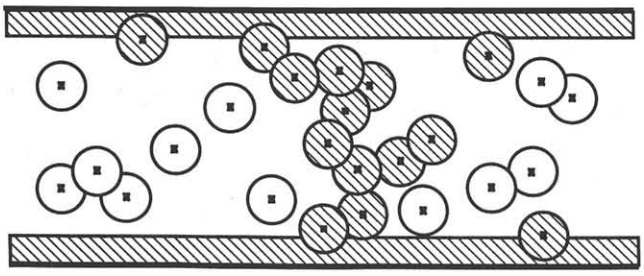

Fig.7 Schematic illustration of the model for intrinsic oxide breakdown based on electron trap generation. The spheres correspond with the interaction region of an electron trap. The conducting local path is indicated by the shaded spheres.

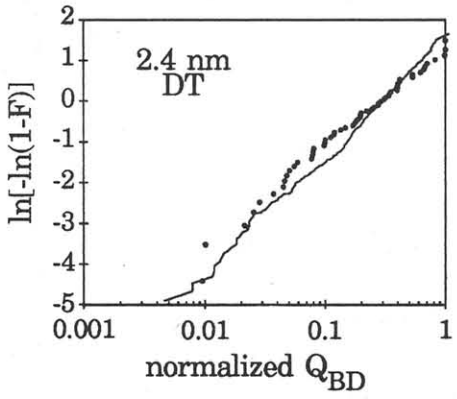

Fig.8 The normalized Q_{BD} distribution of 2.4 nm gate oxide during a constant current stress (0.1 A/cm^2 gate injection) in the DT regime. The symbols are experimental results while the full line is the Monte Carlo simulation of the model [7].

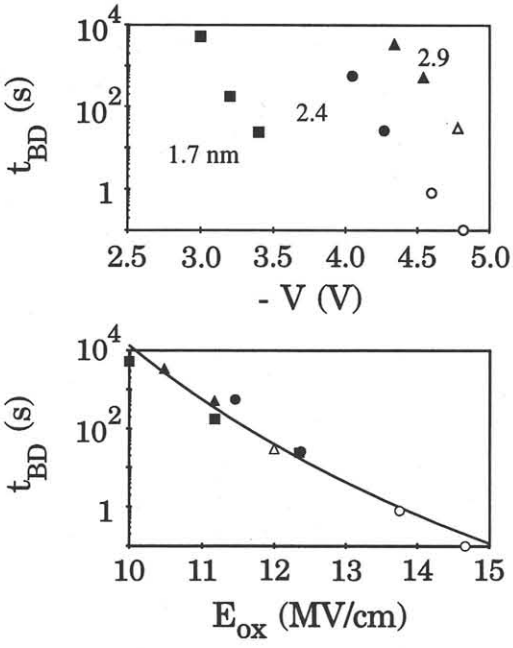

Fig.9 The time to breakdown t_{BD} of ultra-thin (1.7 to 2.9nm) gate oxides as a function of the applied voltage V and the electrical oxide field E_{ox}. The closed and open symbols correspond with a DT resp. FNT stressing. A $1/E_{ox}$ dependence is fitted to the experimental t_{BD} data [8].

In correspondence with [3], a strong increase of the charge to breakdown (Q_{BD}) value is observed in Fig.6 with the transition from a FNT to a DT injection mechanism when a constant current stress is used. This, however, can be explained by the lower oxide field in the case of DT. It is seen in Fig.9 that the time to breakdown t_{BD} (50% value) decreases for thinner oxides at constant voltage. This is explained by the corresponding higher oxide field strength in the thinner oxide. From Fig.9 it is also observed that the TDDB data is only dependent on the oxide field strength while not on the oxide thickness and the tunnel injection mechanism. Our data is in quantitative agreement with the results obtained on thicker (5.2 nm to 10.3 nm) oxides for FNT stress conditions [8]. Using the $1/E_{ox}$ extrapolation model [8], an intrinsic oxide reliability of 20 year is obtained at 7 MV/cm.

4. CONCLUSIONS

It is demonstrated that the growth of extremely uniform ultra-thin 1.5 nm to 3 nm SiO_2 layers on Si can be controlled by thermal oxidation in a low pressure cluster tool furnace. Dielectric breakdown of these ultra-thin gate oxides can occur during direct electron tunneling from the poly-Si gate. Complex fluctuations in the direct tunnel current correspond with the occurrence of dielectric breakdown of these ultra-thin gate oxides. It is also shown that in the direct tunneling regime, the time to dielectric breakdown for these ultra-thin gate oxides is determined by the electrical oxide field strength similar to the case of a Fowler-Nordheim stress. The small slope of the intrinsic Q_{BD} distribution that is observed for these ultra-thin oxide layers in the DT regime can be explained by a statistical model for the electron trap generation.

Acknowledgments

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