Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 785-787

Spatial Distributions of Individual Traps in a Si/SiO_2 Interface

Toshitsugu SAKAMOTO, Hisao KAWAURA, and Toshio BABA
NEC Fundamental Research Laboratories, 34 Miyukigaoka,
Tsukuba, Ibaraki 305, Japan
Phone: +81-298-50-1153 Fax: +81-298-56-6139

We have investigated individual traps in the Si/SiO_2 interface by observing random telegraph signals (RTSs). The traps having energy levels within a few k_BT of the Fermi level can capture or emit single electrons, and become sources of RTSs. We report the first investigation of spatial distributions of single-carrier traps in a MOSFET with a double gate structure. We observe RTSs with changing bias voltages on two lower gates, and show that their variations describe the spatial distributions of the individual traps.

1. INTRODUCTION

The Si/SiO_2 interface or thermally oxidized silicon contains many kinds of traps or charges such as interface traps and fixed oxide charges. These traps or charges play a crucial role in device operations. When an empty trap captures a single carrier, either the carrier number in the channel region changes roughly by one or mobility changes since the charged traps become Coulomb scatterers. This variation in carrier number or mobility causes a variation in the source-drain conductance. In a shallow trap, the alternate capture and emission of carriers causes telegraph switching of the output at random intervals. These signals are known as random telegraph signals (RTSs).[1-4] Since device miniaturization reduces the number of electrons in the active region, even a single trap can significantly degrade device performance. Thus, it has become increasingly important to characterize the traps.

Although processing technology has improved significantly, traps and their production mechanisms are not yet completely understood. Various electric-transport methods have been investigated for carrier traps. Capacitance transients have been used to determine the thermal activation energy of the trap level as well as its concentration.[5] Another electronic measurement method has been investigated by Ralls *et al.* which uses RTSs caused by capture and emission of a single carrier at the trap in the Si/SiO_2 interface.[2] The temperature dependence of the dwell time reveals thermal activation energy for individual trapping. In these experiments, only the traps beneath the gate region were measurable; their spatial locations could not be determined.[1-4]

In this contribution we demonstrate that the locations of the traps in the Si/SiO_2 interface can be determined by observing RTSs. We identify 3 traps and their positions. We also estimate the thermal activation energy for each trap from temperature dependence of the dwell time.

2. EXPERIMENTAL RESULTS

Our device is a double gate, n-channel Si-MOSFET where a narrow channel can be defined electrically. Figure 1 shows a schematic view of the device. The Si(100)/SiO_2 interface was defined by thermal process at 950 °C. A poly-Si lower gate and a Ti/Au upper gate are separated by a 70 nm CVD-SiO_2 layer. Annealing was carried out in H_2 at 450 °C after CVD. The upper gate, positively biased to V_U = 0.6 V, induces an inversion layer in p-type Si substrate. Two lower gates, biased to V_{L1} and V_{L2} respectively, form the narrow channel in the inversion layer. The width and length of the slit between in the two lower gates are about 0.3 μm and 0.1 μm respectively. The current was measured with a constant source-drain voltage of 3.0 mV at a temperature of 4.5 K.

The current through the narrow channel is measured with changing V_{L2} for fixed V_{L1} = -5.0 V (Figure 2). The current oscillates aperiodically with V_{L2}. Temperature dependence of the oscillations and I-V characteristics reveal that successive increments of single electrons into conducting islands causes aperiodic Coulomb blockade.[6] These islands may be formed by potential fluctuations due to the charged traps in the vicinity of the Si/SiO_2 interface. Besides these oscillations, current "bumps" occur at several voltages (V_{L2} = -5.36 and -4.66 V), interrupting the smooth characteristics. At the "bumps", the current spontaneously

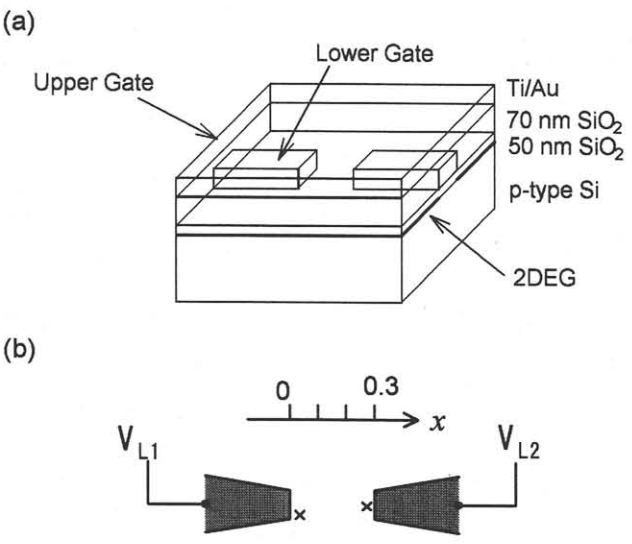

Figure 1. (a) Schematic view of a double gate, n-channel MOSFET. (b) Schematic top view of lower gate. Cross marks show the traps in the interface of Si/SiO_2.

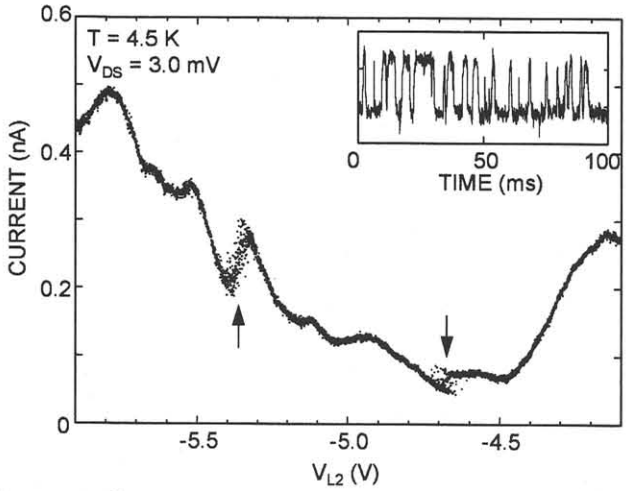

Figure 2. Current through narrow channel with changing V_{L2} for V_{L1} = -5.0 V. Sweeping rate of V_{L2} is 0.25 V/min. Random telegraph signals are observed at V_{L2} = -5.36, -4.66 V (shown by arrows). Inset: Time dependence of the current at V_{L2} = -5.85 V.

switches between two current states with random intervals (inset, Figure 2). The average dwell time $<\tau_{high}>$ in the high current state or $<\tau_{low}>$ in the low current state is several milliseconds. This signal is known as a random telegraph signal (RTS). These RTSs comprise two kinds of fluctuations. One is the fluctuation in the phase of CB oscillations. The total island charge changes by a fractional charge induced by the trapped charge. The other fluctuation is in the amplitude of the CB oscillations. The trapped charges modify the potential height of the tunnel barrier by their Coulomb potential, resulting in the variation of the tunnel conductance. The CB effect makes the RTSs large enough to overcome measurement noise level. The RTS amplitude relative to the total current reaches up to 30 % and 36 % for RTS at V_{L2} = -5.36 V and at -4.66 V, respectively.

Slower trappings than sweeping rate of V_{L2} may cause a steplike change in the current and even cause hysterisis characteristics in the current for up and down sweeping of V_{L2}. These slow trappings stochastically change the gate voltages where RTS occurs. In the present measurement, we did not observe such slow trappings. However, in other samples slow trappings were frequently observed and made characterizing individual traps difficult since the gate voltages at RTS changed for each sweeping of gate voltage.

We also measured the current through the narrow channel with changing V_{L1} for various V_{L2} (Figure 3(a)). The points where the current fluctuations are larger than measurement noise level (14 pA) are plotted in a (V_{L1}, V_{L2}) plane (Figure 3(b)). This clearly shows the distributions of RTSs. The (V_{L1}, V_{L2}) values at RTSs are related to the energy levels of the traps. The set of points, which consists of RTSs caused by a specific trap, forms a line in the (V_{L1}, V_{L2}) plane. Each line has a different dependence on V_{L1} or V_{L2}. For RTS #1, small changes (ΔV_{L1}) in V_{L1} from the initial position, for example, (V_{L1}, V_{L2}) = (-5.0, -4.66 V) do not affect the occurrence of RTS; however, small changes (ΔV_{L2}) of V_{L2} cause the RTS to disappear. This indicates that the energy level of the trap, causing RTS #1, is easily shifted by V_{L2} rather than V_{L1}. These variations sugg-

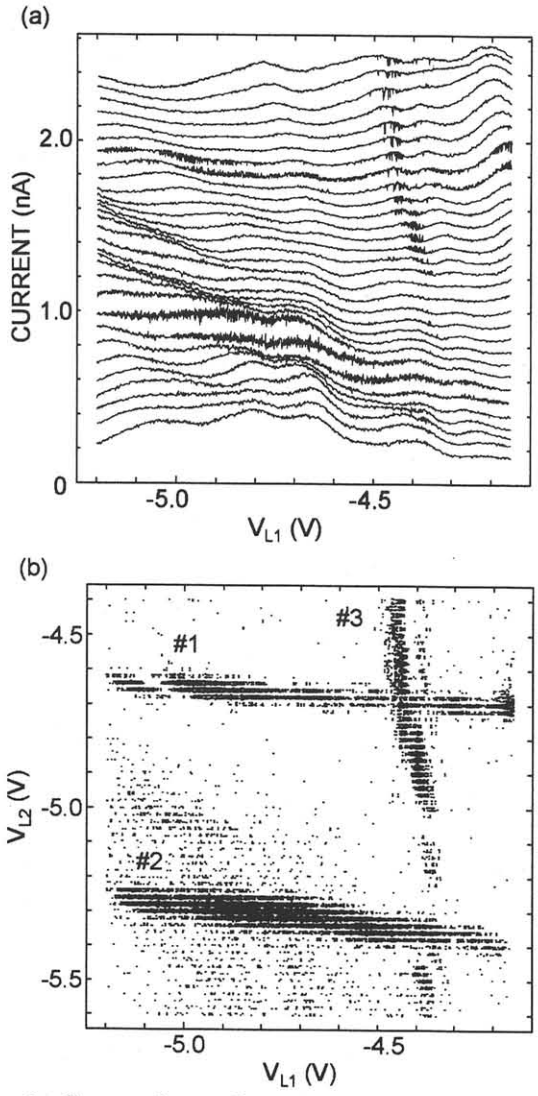

Figure 3. Gate voltage dependence of RTSs. (a) Current versus V_{L1} for equally spaced V_{L2} from -4.4 (top) to -5.6 V (bottom). Each curve is offset for clarity. (b) Points where current fluctuations are larger than 14 pA are plotted as a function of V_{L1} for different V_{L2}. RTSs are indicated by the dense clouds of points.

gest that the trap causing RTS #1 exists near gate L2. Here, RTS #2 shows the same behavior as RTS #1, and the trap causing RTS #2 also exists near gate L2. On the other hand, the trap level causing RTS #3 change drastically when V_{L1} is varied, and is insensitive to V_{L2}. This shows that the trap causing RTS #3 exists near gate L1.

At the intersection of RTS #1 and #3 ((V_{L1}, V_{L2}) = (-4.44, -4.68 V)), three level RTSs were observed. In contrast to prior experiments[1,7], there was no correlation between the two RTSs. This suggests that the trap causing RTS #1 is located far from the trap causing RTS #3 and supports the above explanations.

3. DISCUSSION

As mentioned in the previous section, the slope of the line ($\Delta V_{L2}/\Delta V_{L1}$) in Fig. 3(b) shows the sensitivity of the trap level for the variation in V_{L1} or V_{L2}. We will estimate the x position of the traps from this slope us-

ing a simple model, where x is the direction perpendicular to the narrow channel (Fig. 1(b)). We assume that the variation in the conduction band along the x axis in the slit depends linearly on V_{L1} or V_{L2}; the variation in the trap level linearly depends on the distance from the gate to the trap. For the first order approximation, this assumption is valid for our system. The distance x from the gate L1 to the trap can be given by

$$\frac{x}{W-x} = \frac{\Delta V_{L1}}{\Delta V_{L2}},$$

where W is the width of the slit, which is 0.3 μm for our device. The estimated values are listed in Table 1.

Traps are located near the lower gate. Since the potential change near the gate is larger than that in the center of the slit when the gate electrode is biased negatively, the traps near the gate are preferably observed. Here, the y positions of the traps are not clear. Another split gate will give additional information about the y positions of the traps.

Table 1. Measured parameters (defined in text) of individual traps.

RTS No.	x (μm)	ΔE_{high}(meV)	ΔE_{low}(meV)
#1	0.28	2.9	2.5
#2	0.27	1.0	1.0
#3	0.02	< 1.0	< 1.0

Each RTS has its own characteristic activation energy, which defines the dwell times of RTS and the observation temperature range. In the same manner as Rall's experiment[3], $<\tau_{high}>$ and $<\tau_{low}>$ for RTS #1-3 depends exponentially on inverse temperature. From the slope of such plots, the activation energy is given by

$$\Delta E_{high,low} = \frac{d\, ln < \tau_{high,low} >}{d\left(1/k_B T\right)}.$$

The obtained values are also listed in Table 1. As far as we know, a trap whose activation energy is of the order of several meV in a Si/SiO_2 interface has not yet been reported. Lower temperature measurement can confirm the traps with lower activation energies.

4. CONCLUSION

Individual traps in the Si/SiO_2 interface have been studied by observing random telegraph signals in a double gate, n-channel Si-MOSFET. We found 3 traps within the 0.3 μm slit between two lower gates, and they have a characteristic dependence on the gate bias on the lower gate. The dependences of the trap levels on the gate voltages reveal the x positions of the individual traps. The activation energy of each trap was also estimated from the temperature dependence of its dwell time.

We would like to thank Jun'etsu Sone for Si fabrication, Yukinori Ochiai for his help in EB lithography, and Kazuo Nakamura and Jun'ichi Sone for their continuous encouragement. This work was performed under the management of FED as a part of the MITI R&D of Industrial Science and Technology Frontier program (Quantum Function Devices Project) supported by NEDO.

REFERENCES

1) M. J. Kirton and M. J. Uren, Advan. Phys. 38 (1989) 367.
2) K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth and D. M. Tennant, Phys. Rev. Lett. 52 (1984) 228.
3) M. J. Kirton and M. J. Uren, Appl. Phys. Lett. 48 (1986) 1270.
4) M. J. Kirton, M. J. Uren, S. Collins, M. Schulz, A. Karmann, and K. Scheffer, Semicond. Sci. Technol. 4 (1989) 1116.
5) D. V. Lang, J. Appl. Phys. 45 (1974) 3023.
6) J. H. F. Scoott-Thomas, S. B. Field, M. A. Kastner, H. I. Smith, and D. A. Antoniadis, Phys. Rev. Lett. 62 (1989) 583.
7) T. Sakamoto, Y. Nakamura, S.W. Hwang, and K. Nakamura, Jpn. J. Appl. Phys. 34 (1995) 4302.