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Demonstration of an Electronic Grade Ti/AlN/Si Metal-Insulator-Semiconductor Capacitor

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AlN has been grown on Si(111) substrates by metalorganic chemical vapor deposition. A metal-insulator-semiconductor (MIS) structure was fabricated using the AlN layer as the insulator. For the first time, the interface trap level density distribution in the upper half bandgap of n-type Si was calculated from high-low frequency capacitance-voltage and conductance-voltage measurements. The interface trap level density was in the range of 1×10^{11} to $7\times10^{11}cm^{-2}eV^{-1}$. An electronic-grade AlN and AlN/Si interface have been successfully demonstrated.

1. Introduction.

The realization of high brightness blue, green and yellow light emitting diodes (LEDs) from InGaN, GaN and AlGaN[1] has stimulated tremendous scientific interest in these large bandgap (1.9eV to 6.2eV) III-Nitride semiconductors. In fact, the applications of these materials are not limited to LEDs and laser diodes. They are also promising for high power and high frequency electronic devices due to their potential advantages such as high electric breakdown strength, small leakage current, high chemical stability and radiation hardness. High performance GaN/AlGaN heterojunction field-effect transistors (FETs) operating up to 70GHz have been reported[2]. Metal-insulator-semiconductor (MIS) FET using AlN as the gate dielectric on Si has also been demonstrated[3].

Silicon-based nitride epitaxy is promising for co-integration of wide band-gap optoelectronic devices with large scale circuits employing silicon FETs. For example, AlN is a good insulator due to its large bandgap (6.2eV). Comparing with the traditional SiO_2/Si MOS system, AlN/Si system offers several advantages. First, monocrystalline AlN can be grown on Si[4-8] which has the potential to provide a better quality, oxygen-free interface. Secondly, AlN can be p- or n-type doped[9] and heterojunctions can be formed using the $Al_xGa_{1-x}N$ material system, which is very promising for fabricating various electronic device structures. The AlN/Si interface plays a key role in device performances. Various researchers have characterized the AlN/Si interface using capacitance-voltage(C-V) and conductance-voltage (G-V) measurements[10-12]. However, because of the poor quality of the AlN layer (polycrystalline or amorphous), leakage current was high. As a result, the high-frequency C-V performance of the MIS structure was poor; the low-frequency C-V has never been reported and thus the minority carrier response at the interface has been unknown. The distribution of the interface trap level density across the Si bandgap has not been reported either.

In this paper, we report the characterization of AlN/Si(111) interface using a MIS structure in which AlN is the insulator grown by metalorganic chemical vapor deposition (MOCVD). For the first time, we demonstrate both the high and low frequency C-V performance of the MIS structure. From C-V and G-V measurements, the interface trap level density in the upper half bandgap of n-type Si is also given.

2. Experiments.

The growth conditions of AlN on Si(111) substrates were basically the same as what we have reported for the growth of high quality AlN on sapphire using MOCVD[13]. Briefly, Trimethylaluminum (TMAl) and ammonia (NH_3) were used as starting materials for Al and N elements respectively. The carrier gas was hydrogen. The growth temperature was 1000°C, and the reactor pressure was 100 mbar. The substrate was dipped into diluted HF solution to remove oxidation and was transferred into the reactor immediately after the dip. Then it was heated up to 1100°C under H_2 for further cleaning. After that, the reactor temperature was lowered to 1000°C and TMAl and NH_3 were introduced to the reactor to start AlN growth. The epilayers typically show a mirror like morphology. The full-width at half-maximum of the X-ray rocking curve is typically around 10 arcmins. The samples were also characterized by Fourier transform infrared (FTIR) spectroscopy.

The Si(111) substrate is n-type with an electron carrier concentration of $1.26\times10^{15}cm^{-3}$. The AlN epilayer has a thickness of 780Å, which is measured with the cross-section SEM. To fabricate the top metal contact on AlN, a 2000Å-thick Ti/Au layer (AlN/Ti(500Å)/Au(1500Å)) was first evaporated on the whole surface in an electron-beam vacuum evaporator and then contacts with dimensions of 400μm×400μm were formed using a standard photolithography procedure. The distance between these contacts was 250μm. The back contact on Si was indium. I-V curves between two isolated indium contacts confirmed that they were very good ohmic contacts. I-V curves between the top Ti/Au contacts and the back indium contacts showed that the leakage current at gate bias of 6V is less than 1nA. No other processing was performed before the measurements were carried out in this report. Some constants used in the calculation are: (i) The relative dielectric constant of AlN $\varepsilon_i = 9.4$; (ii) The electron affinity and bandgap energy of Si, $\chi_S = 4.15eV$ and $E_g = 1.12eV$ respectively; (iii) the work function of Ti $W_M = 4.319eV$. Thus the capacitance of the AlN layer is calculated as $C_i = 1.037\times10^{-7}F/cm^2$. The work function difference between Ti and Si is $\psi_{MS} = -0.097eV$. It is expected that the effect of such a small work function difference on the C-V measurements is very small.

C-V and G-V measurements were performed at room temperature in darkness, with a DC gate bias and a small AC signal. These measurements were done with a Hewlett-Packet 4192A LF impedance analyzer controlled by a computer. The top contact was connected to the positive electrode.

3. Results and Discussion.

Figure 1 is the FTIR transmittance of the AlN/Si (111) used in this experiment, which was obtained from a Mattson Galaxy 3000 FTIR spectrometer at room temperature with background calibration. The sharp phonon mode at $665cm^{-1}$ corresponds to one of the TO phonon modes of AlN indicating the good quality of the epilayer. No other modes were detected within the limit of the instrument.

Figure 2 shows the C-V curves at 50Hz, 1kHz, 10kHz and 100kHz. The capacitance has been normalized to the insulator capacitance $C_i = 1.037\times10^{-7}F/cm^2$. In the figure, at large positive gate bias, the Ti/AlN/n-Si MIS structure is in the accumulation region, in which the C-V characteristics of the MIS structure is determined by the majority carriers (electrons) accumulated in the space-charge region. The response of the majority carriers is very fast thus the capacitance is frequency-independent. At negative bias, majority carriers are depleted from the space-charge region while minority carriers (holes) begin to accumulate in this region. The response of the minority carriers is slow so a frequency-dependent C-V characteristics is observed. To our knowledge, this is the first time that inversion is observed for both high and low frequencies. The maximum/minimum capacitance ratio as high as $C_{max}/C_{min} = 9$ was achieved for the measured frequency range. These results indicate the high quality of the AlN and AlN/Si interface.

The interface trap level density was calculated with two methods. One is the high-low frequency method[14)] and the other is conductance method[14,15)]. In the high-low frequency method, 50Hz (C_{LF}) and 100kHz (C_{HF}) C-V were

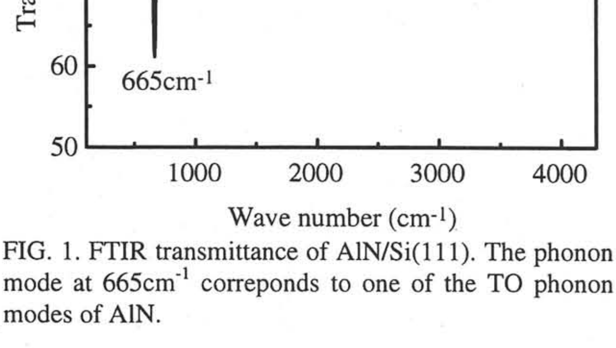

FIG. 1. FTIR transmittance of AlN/Si(111). The phonon mode at $665cm^{-1}$ correponds to one of the TO phonon modes of AlN.

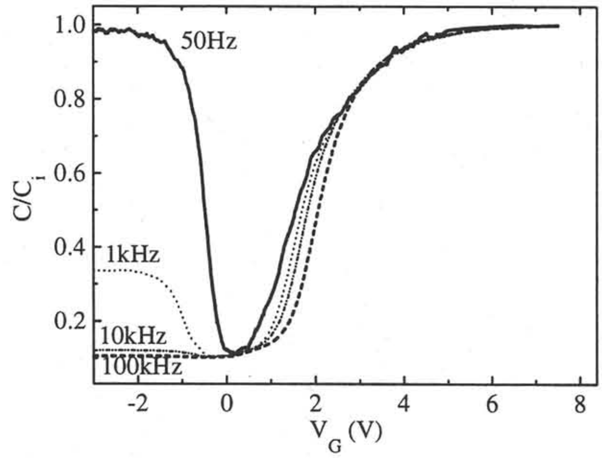

FIG. 2. C-V curves of the AlN/Si MIS structure at different frequencies: 50Hz, 1kHz, 10kHz and 100kHz.

used as the low and high-frequency data respectively. Then the capacitance of the interface trap charges C_{it} at gate bias V_G was calculated by

$$C_{it}(V_G) = \left(\frac{1}{C_{LF}(V_G)} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}(V_G)} - \frac{1}{C_i}\right)^{-1} \quad (1)$$

In the conductance method, the conductance of the MIS structure G_m was measured as a function of AC signal frequency ω at a fixed gate bias V_G. Then the ratio of the parallel conductance of the interface charge admittance in the equivalent circuit to frequency ω was calculated as

$$\frac{G_p}{\omega} = \frac{\omega C_i^2 G_m \left(G_m^2 + \omega^2 C_m^2\right)}{\omega^2 C_i^2 G_m^2 + \left[\omega^2 C_m (C_i - C_m) - G_m^2\right]^2} \quad (2)$$

G_p/ω was plotted against ω at each gate bias. The peak value of the plot gave $C_{it}(V_G)/2$. In both methods, after $C_{it}(V_G)$ was found, the interface trap level density $D_{it}(V_G)$ was calculated as $D_{it}(V_G) = C_{it}(V_G)/q$, where q is the electron charge.

The band-bending at different biases was determined from the 50Hz C-V curve as follows. First, the flat-band capacitance at low frequency was calculated with standard MIS theory[14-16)] to be $C_{FB} = 4.835\times10^{-8}F/cm^{-2}$ (at V_G=0 theoretically), which gives $C_{FB}/C_i = 0.466$. From this value and the 50Hz C-V curve, it was found that the experimental flat-band voltage $V_{FB} = 1.46V$. Then the band-bending $\psi_S(V_G)$ was calculated as[14,15)]:

$$\psi_S(V_G) = \int_{V_{FB}}^{V_G} dV_G \left(1 - \frac{C_{LF}(V_G)}{C_{ox}}\right) \quad (3)$$

since $\psi_S(V_{FB}) = 0$. From $V_{FB} = 1.46V > 0$, it can be derived that the interface traps are mainly of the acceptor type.

Figure 3 shows the interface trap level density at different band-bending obtained from both methods. Here $\psi_S > 0$ corresponding to a downward band-bending (towards valence band). It can be seen that the results given by both methods are approximately similar. The lowest distribution ($<1\times10^{11}cm^{-2}eV^{-1}$) is closest to the midgap and the highest distribution ($7\times10^{11}cm^{-2}eV^{-1}$) is at approximately 0.3eV above the valence band of Si. The interface trap level density is approaching to that of unprocessed SiO_2/Si system and comparable to that of the AlN/Si interface obtained by other authors[10-12]. The deviation of the interface trap level density in or near inversion ($\psi_S < 0$) given by the two different methods is mainly due to the limitation of the high-low frequency method as pointed out by Nicollian *et.al*[15]. In or near inversion, the minority carriers do not follow the high frequency gate bias so equation (1) is not valid, while the conductance method has no such limitation and can give more accurate interface trap level density [14,15].

4. Conclusions.

In conclusion, epitaxial AlN was grown on Si (111) substrates using MOCVD. The AlN/Si interface was characterized by high-low frequency C-V measurements and G-V measurements at different frequencies. The interface traps are_mainly of the acceptor type. Its density is in the range of 1×10^{11} to $7\times10^{11}cm^{-2}eV^{-1}$, and the highest density is around 0.3eV above the valence band. Maximum/minimum capacitance ratio as high as 9 has been achieved. An electronic-grade AlN and AlN/Si interface have been successfully demonstrated without any post-growth processing.

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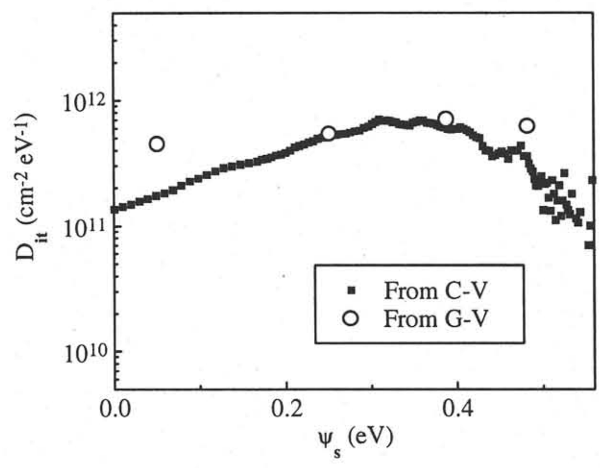

FIG. 3. Interface trap level density distribution in the upper half bandgap of n-type Si. Results obtained using high-low C-V and G-V methods are shown respectively.

References

1) S. Nakamura, M. Senoh, N. Isawa and S. Nagahama, Jpn. J. Appl. Phys. **34** (1995) L797.
2) M. A. Khan, Q. Cheng, C. J. Sun, J. Yang and M. S. Shur, The First International Symposium on Gallium Nitride and Related Materials, MRS Fall Meeting Symposium AAA, Boston, MA, December, 1995, Paper **AAA13.2.** (to be published).
3) S. Stevens, M. Kinniburgh,, A. F. Schwartzman, A. Ohtani and R. Beresford, Appl. Phys. Lett. **66** (1995) 3197.
4) S. Stevens, A. Ohtani, M. Kinniburgh and R. Beresford, Appl. Phys. Lett. **65** (1995) 321.
5) M. Miyauchi, Y. Ishikawa and N. Shibata, Jpn. J. Appl. Phys. **31** (1992) L1714.
6) M. Morita, S. Isogai, N. Shimizu, K. Tsubouchi and N. Mikoshiba, Jpn. J. Appl. Phys. **20** (1981) L173
7) P. Kung, A. Saxler, X. Zhang, D. Walker, T. C. Wang, I. Ferguson and M. Razeghi, Appl. Phys. Lett. **66** (1995) 2958.
8) X. Zhang, P. Kung, A. Saxler, D.Walker, T. C. Wang and M. Razeghi, Appl. Phys. Lett. **67** (1995) 1745.
9) K. Wongchotiqul, N. Chen, D. P. Zhang, X. Tang and M. G. Spencer, The First International Symposium on Gallium Nitride and Related Materials, MRS Fall Meeting Symposium AAA, Boston, MA, December, 1995, Paper **AAA5.5.** (to be published).
10) S. Mirsch, H. Reimer, Phys. Status Solidi. **A11**(1972).631
11) J. J. Hantzpergue, Y. Pauleau, J. C. Remy, D. Roptin and M. Cailler, Thin Solid Films **75** (1981) 167.
12) E. A. Irene, V. J. Silvestri and G. R. Woolhouse, J. Electronic Mater. **4** (1975) 409.
13) A. Saxler, P. Kung, C. J. Sun, E. Bigan and M. Razeghi, Appl. Phys. Lett. **64** (1994) 339.
14) E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, (Wiley, New York, 1982).
15) E. H. Nicollian and A. Goetzberger, Bell. Syst. Tech. J. **46** (1967) 1055.
16) S. M. Sze, Physics of Semiconductor Devices (Wiley, New York, 1981), 2nd ed., Chapter 7.