Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 94-96

InGaP/GaAs Sub-Square-Micron Emitter HBT with f_{max}>100 GHz

Koji HIRATA, Tomonori TANOUE*, Hiroshi MASUDA*, Hiroyuki UCHIYAMA* and Akihisa TERANO*
Hitachi ULSI Engineering, Corp.,
5-20-1 Josuihon-cho, Kodaira, Tokyo 187, Japan
*Central Research Laboratory, Hitachi Ltd.,
1-280 Higashi-Koigakubo, Kokubunji, Tokyo 185, Japan

InGaP/GaAs HBTs with a sub-square-micron emitter have been fabricated using a novel self-aligned emitter etching process. They exhibited a high current gain of 44 for an emitter size of 0.4 x 1.7 μm^2. Furthermore, excellent microwave performances, i.e., an f_T of 62 GHz and f_{max} of 105 GHz for an emitter size of 0.4 x 2.2 μm^2 were obtained. This f_{max} is the highest value ever reported for GaAs-based HBTs with an emitter area of less than 1 μm^2.

1. Introduction

InGaP/GaAs HBTs are conceivable next-generation devices to succeed AlGaAs/GaAs HBTs because of their high-reliability.[1,2] and they have been considered the most promising devices for high-speed integrated circuits applications[3] or microwave power application.[4] However, in conventional InGaP/GaAs HBTs, the spacing between the emitter mesa and the base ohmic contact is obtained by side etching during the emitter etching process.[1] Because of the poor controllability of the isotropic side etching, this process causes serious problems when one tries to reduce the emitter size.

In this paper, we report a novel self-aligned emitter etching process, and present DC and AC characteristics of the fabricated InGaP/GaAs HBTs with a sub-square-micron emitter.

2. Device Structure and Fabrication Process

The epitaxial layers were grown on a semi-insulating GaAs (100) substrate by MOCVD, using Si and C for n-type and p-type dopants, respectively. The layer structures are summarized in Table I.

Table I. Epitaxial layer structure of the fabricated InGaP/GaAs HBT.

Layer	Material	Thickness (nm)	Doping (cm^{-3})
Cap	$In_xGa_{1-x}As$ (x=0 - 0.6)	80	Si:$5x10^{18}$- $3x10^{19}$
	GaAs	50	Si:$5x10^{18}$
Emitter	$In_xGa_{1-x}P$ (x=0.5)	20	Si:$5x10^{18}$
	$In_xGa_{1-x}P$ (x=0.5)	30	Si:$5x10^{17}$
Base	GaAs	30	C:$4x10^{19}$
Collector	GaAs	200	Si:$1x10^{16}$
Sub collector	GaAs	500	Si:$5x10^{18}$
Substrate	S. I. GaAs		

The schematic cross section of the self-aligned InGaP/GaAs HBT is shown in Fig. 1. In our process, the emitter mesa was formed by a self-aligned process using electron cyclotron resonance (ECR) etching and selective wet chemical etching.

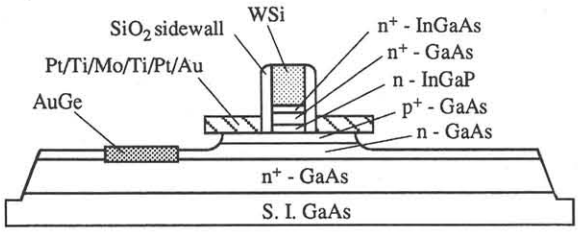


Fig. 1. Schematic cross section of the self-aligned InGaP/GaAs HBT.

First, the WSi emitter electrode was defined by ECR etching using a mixture of CHF_3 and SF_6. Then, the InGaAs and GaAs cap layers were etched by ECR plasma of a Cl_2 and CH_4 gas mixture, using the emitter electrode as a mask, the etch pressure was 0.24 mTorr, and the microwave and RF powers were 100 W and 80 W, respectively. This etching achieved a vertical emitter mesa shape. Moreover, the etching depth in the InGaAs/GaAs/InGaP multilayer was controlled by end-point detection technique, monitoring 470 nm-light induced by the reaction between Cl and In (Fig. 2). After this dry etching, the InGaP emitter layer was selectively etched from the GaAs base layer by wet chemical etching using the cap layers as a mask.

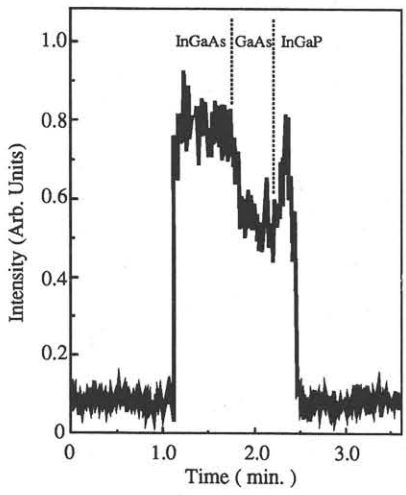


Fig. 2. End-point detection during emitter etching of the multilayer in InGaAs/GaAs/InGaP.

Next, SiO_2 sidewall was formed by chemical vapor deposition (CVD) and subsequent etching-back process using

reactive ion etching. The Pt/Ti/Mo/Ti/Pt/Au base electrode was formed by a lift-off technique on the p^+-GaAs base layer. Unnecessary Pt/Ti/Mo/Ti/Pt/Au film on the emitter electrode was removed by another etching-back method. The base mesa was formed by wet chemical etching using the base electrode as a mask. AuGe collector electrode was formed by a lift-off technique after the subcollector layer was exposed by wet-etching. Both the base and collector electrodes were simultaneously alloyed at 350°C for 30 minutes in N_2 ambient. Finally, the active devices were isolated by wet-etching. The SEM cross-sectional view of the InGaP/GaAs HBT is shown in Fig. 3. A 0.3-μm wide SiO_2 sidewall was used to separate the emitter electrode from the base electrode.

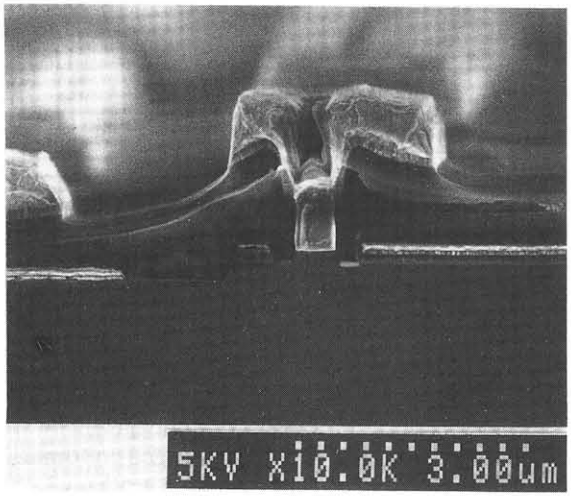


Fig. 3. Cross-sectional SEM photograph of the fabricated InGaP/GaAs HBT.

3. Results and Discussion

Gummel plot of the fabricated InGaP/GaAs HBT with the smallest emitter size of 0.4 x 1.7 μm^2 showed a high current gain of 44 (Fig. 4). The ideality factor n of the collector current is unity, and the base current showed two ideality factors n of 1.9 and 1.2 at the low and high current levels, respectively.[5,6] This indicates that the ECR etching processes have not left noticeable damage in the device.

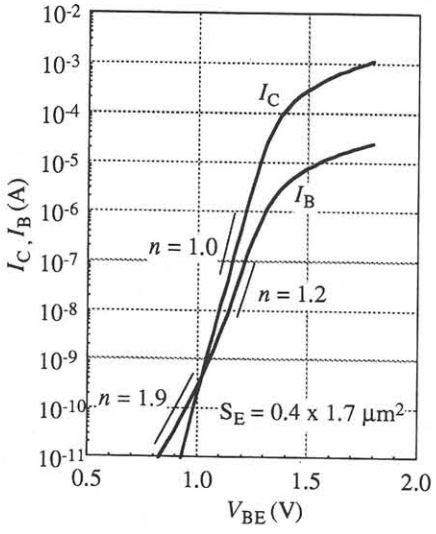


Fig. 4. Gummel plot of the self-aligned InGaP/GaAs HBT.

In Fig. 5, the dependence of current gain on emitter-base junction size for InGaP/GaAs HBTs is compared with that for AlGaAs/GaAs HBTs having a similar device structure. Two types of device structures were fabricated for AlGaAs/GaAs HBTs. One had a thin emitter layer on the extrinsic base layer, preventing surface recombination in the extrinsic base region. The other had no thin emitter layer. Although the InGaP/GaAs HBTs also did not have a thin emitter layer on the extrinsic base, its emitter size dependence on current gain was close to that of the AlGaAs/GaAs HBT that did have a thin emitter layer on the extrinsic base. This can be attributed to a low surface recombination at the InGaP emitter periphery.[6,7] This dependence, although small, for InGaP/GaAs HBT will further be improved by using a thin emitter layer on the extrinsic base.[8] Our end-point detection technique in the ECR etching should be advantageous for fabricating the device with the thin emitter layer.

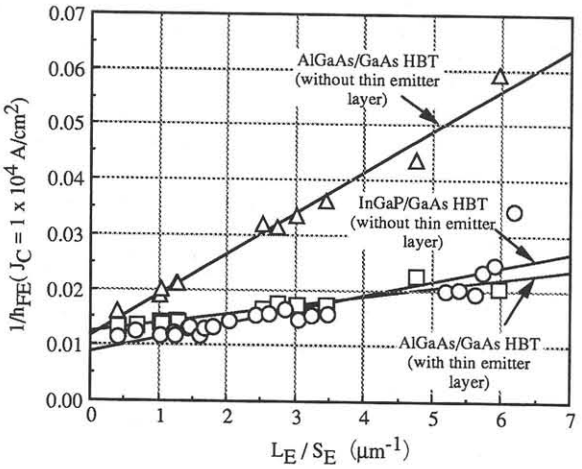


Fig. 5. Dependence of current gain on size of emitter-base junction in InGaP/GaAs HBTs compared with AlGaAs/GaAs HBTs.

Figure 6 shows the dependencies of cutoff frequencies f_T and maximum oscillation frequencies f_{max} on collector current at V_{CE} = 1.6 V for HBTs with different emitter sizes.

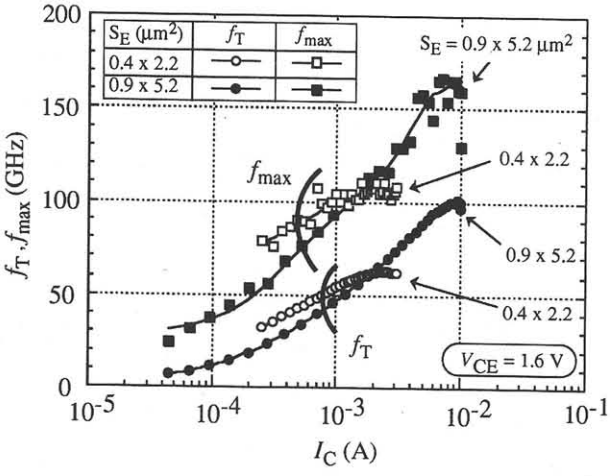


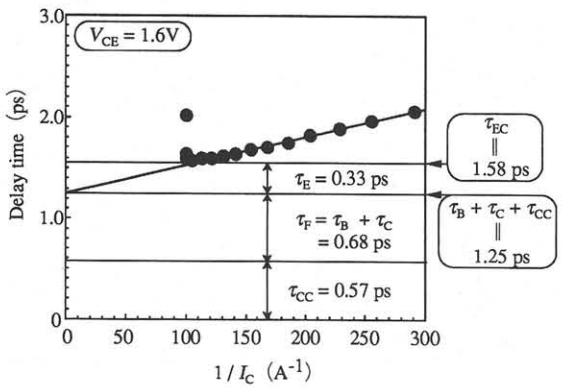
Fig. 6. f_T , f_{max} versus I_C of self-aligned InGaP/GaAs HBTs at V_{CE}=1.6V.

The high values of f_T = 101 GHz and f_{max} = 160 GHz were obtained for an emitter size S_E of 0.9 x 5.2 μm^2. For the HBT with a smaller S_E of 0.4 x 2.2 μm^2 were achieved an f_T of 62 GHz and an f_{max} of 105 GHz. This f_{max} value is the highest ever reported for the sub-square-micron emitter HBTs fabricated on GaAs substrate. It should be noted that the performance of the device with S_E = 0.4 x 2.2 μm^2 exceeded that of the device with S_E = 0.9 x 5.2 μm^2 at I_C lower than 1.5 mA despite the reduction in peak f_T and f_{max}. The f_{max} reached 100 GHz at I_C as low as 1.0 mA.

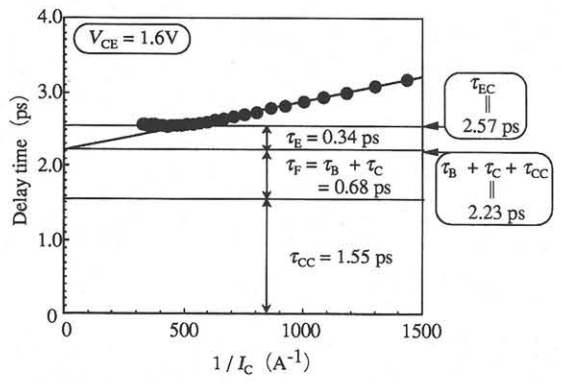
The delay times in these devices were analyzed by the $1/(2\pi f_T)$ versus $1/I_C$ curve, as shown in Fig. 7. The total delay time τ_{EC} is expressed by

$$\tau_{EC} = \tau_E + \tau_B + \tau_C + \tau_{CC} = 1/(2\pi f_T), \quad (1)$$

where τ_E, τ_B, τ_C, and τ_{CC} are the emitter charging time, base transit time, collector transit time, and collector charging time, respectively. The observed f_T of 101 GHz and 62 GHz correspond to the total delay time of 1.58 ps and 2.57 ps , respectively. The τ_E was determined by extrapolating the $1/(2\pi f_T)$ versus $1/I_C$ curve to $1/I_C = 0$. The τ_B and τ_C should be the same because of the same epitaxial structure.



a) emitter size 0.9 x 5.2 μm^2



b) emitter size 0.4 x 2.2 μm^2

Fig. 7. $1/(2\pi f_T)$ versus $1/I_C$ curve of self-aligned InGaP/GaAs HBT.

Therefore, the τ_{CC} of the 0.4 x 2.2 μm^2 device is 0.98 ps larger than that of the 0.9 x 5.2 μm^2 device. This τ_{CC} is expressed by

$$\tau_{CC} = (R_{EE} + R_C) C_{BC}, \quad (2)$$

where R_{EE} and R_C are the emitter series and collector resistances, respectively, and C_{BC} is the base-collector capacitance. From the device parameters shown in Table II, it is clear that the increase of τ_{CC} in the 0.4 x 2.2 μm^2 device is mainly attributed to the increase in R_{EE}. These results indicate that a reduction in emitter resistance is essential to achieve higher microwave performance in an HBT with a sub-square-micron emitter.

Table II. Device parameters.

S_E (μm^2)	0.4 x 2.2	0.9 x 5.2
R_{EE} (Ω)	125	20
R_C (Ω)	16	10
C_{BC} (fF)	11	19

4. Conclusions

We have developed a novel self-aligned emitter etching process which combines anisotropic dry etching, end-point detection technique and wet selective etching for InGaP/GaAs HBTs. This process is very successful in reducing the emitter size with its high etching controllability and uniformity. The fabricated HBT with an emitter size of 0.4 x 2.2 μm^2 achieved an f_T of 55 GHz and an f_{max} of 100 GHz at I_C = 1.0 mA and a peak f_T of 62 GHz and a peak f_{max} of 105 GHz. These results indicate that InGaP/GaAs HBTs are very promising for high-speed HBT ICs with extremely low power consumption.

References

1) T. Takahashi, S. Sasa, A. Kawano, T. Iwai and T. Fujii, International Electron Devices Meeting Digest (1994) 191.

2) S. R. Bahl, L. H. Camnitz, D. Houng. M. Mierzwinski, J. Turner and D. Lefforge, International Electron Devices Meeting Digest (1995) 815.

3) W. J. Ho, M. F. Chang, A. Sailer, P. Zampardi, D. Deakin, B. McDermott, R. Pierson, J. A. Higgins and J. Waldrop, IEEE Electron Device Lett. **14** (1993) 527.

4) F. Ren, C. R. Abernathy, S. J. Pearton, J. R. Lothian, P. W. Wisk, T. R. Fullowan, Y. K. Chen, L. W. Yang, S. T. Fu, R. S. Brozovich and H. H. Lin, IEEE Electron Device Lett. **14** (1993) 332.

5) W. Liu, Electronics Lett. **27** (1991) 2116.

6) W. Liu and S. K. Fan, IEEE Electron Device Lett. **13** (1992) 510.

7) R. Plana, J. Graffeuil, S. L. Delage, H. Blanck, M. A. di Forte-Poisson, C. Brylinski and E. Chartier, Electronics Lett. **28** (1992) 2354.

8) S. S. Lu and C. C. Huang, IEEE Electron Device Lett. **13** (1992) 214.