Three-Level Charge-Pumping Technique for Grain-Boundary Trap Evaluation in Polysilicon Thin Film Transistors

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Polysilicon thin-film transistor characteristics are evaluated using the three-level charge-pumping (3CP) technique for the first time. By measuring the 3CP current as a function of fall time, the trap state energy distributions at grain-boundaries are obtained for different (electron emission) time constant windows. The 3CP current versus step voltage characteristics show that the change of 3CP currents considerably increase as the fall time decrease. The large change of 3CP current indicates that the large number of trap states (\(D_{gb} \geq 4 \times 10^{11} \text{eV}^{-1}\cdot\text{cm}^{-2}\)) exist in the upper-half of the band gap. As compared to those of the MOSFET's, the time constants of trap states are distributed over the broader range up to 50 \(\mu\text{s}\).

1 INTRODUCTION

Polysilicon thin film transistors (poly-Si TFT's) have recently been investigated due to their application to large area active matrix liquid crystal displays (AMLCD's).\(^1\) Compared with the current amorphous silicon technology, poly-Si TFT's have better device characteristics which will allow for high quality flat panel displays (FPD's).\(^2\) However, poly-Si TFT's performance is limited by the trap states caused by the grain boundaries.\(^3\) Several works of the grain-boundary trap evaluation based on charge pumping technique have been reported so far.\(^4\) In the charge pumping technique, a pulse is applied to the gate of the poly-Si TFT which alternatively fills the trap states with electrons and holes, thereby causing a recombination current to flow in the \(p^+\) contact. The number of trap states may be determined as a function of trap energy by varying the pulse rise and fall times.\(^7\) The weakness of charge pumping method is the difficulty in modeling accurately the transient recombination phenomena occurring during the rise- and fall-time transitions. In order to evaluate the trap state density, major simplification have to be assumed; values of difficult to determine parameters such as the electron- and hole-capture cross sections have to be estimated. To avoid making these approximations, Tseng in 1985 developed the 3CP technique.\(^5\)

In this paper, by adopting the 3CP method in poly-Si TFT, we can obtained the trap state energy distributions for various time constant windows.

2 DEVICE FABRICATION AND EXPERIMENTAL SET-UP

The polysilicon devices used in this study were n-channel TFTs fabricated on initially oxidised quartz substrates by the high temperature process. A 88 nm undoped amorphous-silicon film was deposited by LPCVD and then annealed at 850 °C. After the active regions were defined, a 100 nm LPCVD oxide film was deposited. Then, another polysilicon film was deposited and patterned to be the gate of the device. After defining the gate geometry, self-aligned phosphorus and boron implantations were performed to form the \(n^+\) and \(p^+\) contacts and then, the dopants were activated. All devices were covered with a silicon-nitride film for protection. The threshold voltage and the field effect mobility of the TFT's are 3.7 V and 66 cm\(^2\cdot\text{V}^{-1}\cdot\text{sec}^{-1}\), respectively. The experimental set-up for measuring the 3CP current is illustrated in Fig.1. The plane view of poly-Si TFT and the cross-sectional view along channel width direction are shown in Fig. 1(a) and (b). The source and drain terminals are connected to each other. The gate-voltage waveform are displayed in Fig. 1(c). Periodic staircase-shaped voltage pulses, supplied from a pulse generator, are applied to the gate of the poly-Si TFT whose source/drain \((n^+)\) connected to ground.

![Fig. 1 Schematic diagram of measurement.](image-url)
The 3CP current is measured at the extra body terminal \((p^+\) which is laterally extended beyond the gate electrode in the channel width direction. The \(p^+\) terminal acts as the poly-Si substrate terminal.

3 RESULTS AND DISCUSSION

The 3CP current \(I_{cp}\) flows when the potential is swung from the accumulation condition to the inversion condition.\(^6,^9\) This current is caused by the repetitive recombination of electrons (coming from the source and the drain) and holes (coming from the substrate) at the trap states when the gate drives the channel between inversion and accumulation. A typical 3CP characteristic is shown in Fig. 2 where the 3CP current is plotted as a parameter under the fixed pulse period of 2 ms and step time of 200 \(\mu s\). In order to keep the frequency constant, the accumulation time \(T_{acc}\) is adjusted as the fall time is changed. In the figure, the change of \(I_{cp}\) considerably increase as the fall time decrease. The large change of \(I_{cp}\) indicates that the large number of trap states exist in the upper-half of the band gap. As the energy level moves toward midgap when the step voltage is decreased, the \(I_{cp}\) decreases as seen in Fig. 2 because more trap states will have emptied prior to the final recombination. The grain-boundary trap density \(D_{gb}\) can be obtained by evaluating the step voltage dependence of 3CP current using \(^6,^9\)

\[
D_{gb}(\psi_{step}) = \frac{1}{qfA_g} \frac{dV_{step}}{d\psi_{step}} \frac{dI_{cp}}{dV_{step}},
\]

where \(q, f, A_g, V_{step}, \psi_{step}\) are the electronic charge, frequency of gate pulse, effective gate area, step voltage, and the surface potential, respectively.

To extract the trap density from (1), it is necessary to determine the relationship between surface potential and step voltage. In this study, the surface potential values have been obtained from the field-effect conductance method.\(^10\) With the active layer film thickness, a relationship between step voltage and relative changes in surface potential can be established. Using \(q\psi_{step} - V_{step}\) relationship, we can directly determine \(D_{gb}(\psi_{step})\) from \(I_{cp}-V_{step}\) characteristics. The 3CP current with surface potential is shown in Fig. 3. The surface potential values have been translated such that when step voltage equals the flat band voltage, \(\psi_{step} = 0\). As stated by Tseng\(^3\), the trap density obtained from (1) has the time constant window

\[
T_{fall} < \tau_{ee} < T_{step},
\]

where \(T_{fall}, \tau_{ee}, T_{step}\) are the fall time of gate pulse, electron emission time constant and the step time, respectively. Therefore, by comparing \(I_{cp}-V_{step}\) characteristics, measured using 3CP waveforms with different values of \(T_{fall}\), the number of grain-boundary traps at a given energy level within a particular range of \(\tau_{ee}\) can be determined.

Fig. 4 show the \(D_{gb}(\psi_{step})\) characteristics obtained from (1). The trap densities obtained from 3CP technique are higher than \(4 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}\). From the Fig. 4, it is evident that the large number of trap states with similar \(\tau_{ee}\) exist over a wide range of the upper-band gap energy. As compared to those of the MOSFET's\(^8,^9\), the time constant of trap states are distributed over the broader range up to 50 \(\mu s\).

4 CONCLUSION

The 3CP technique has been adopted for characteriza-

Fig. 2 \(I_{cp}-V_{step}\) characteristics with varying \(T_{fall}\).

\((V_{inv} = 7 \text{ V}, V_{acc} = -10 \text{ V}, V_R = 0.5 \text{ V}, f = 500\)

\(\text{Hz, } T_{rise} = 10 \mu s, \ T_{inv} = 500 \mu s, \ T_{inv-step} = 100 \mu s, \ T_{step} = 200 \mu s)\)

Fig. 3 \(I_{cp}-\psi_{step}\) characteristics. (Mid-gap energy level was referenced as zero)

... and step voltage. In this study, the surface potential values...
Fig. 4 $D_{ph}$-$\psi_{step}$ characteristics. (Mid-gap energy level was referenced as zero)

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