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3D-Technology for Ultra High Density MOS Arrays

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This paper describes a novel approach to reduce the size of MOS memory arrays. Basic idea is to increase the usable chip area by etching long trenches into the silicon surface. The MOS transistors can be placed at the planar areas between the trenches and at the bottom of the trenches. They are vertically isolated by the trench side-walls. Thus, the isolation does not require any net cell area so that the memory cell density can be doubled. We describe test structures for a Read Only Memory (ROM) array and give electrical results. It is shown that the full performance of planar MOS transistors and good isolation characteristics can be achieved with this technology.

1. INTRODUCTION

The integration density of MOS transistor circuits is commonly increased by scaling down the device structure size. In addition to reducing the structure size, a greater device density can be achieved by a new arrangement of the MOS transistors. The regular design of arrays suggests an approach that is based on structuring the semiconductor surface in planar and vertical sections. The planar sections can be used for MOS transistors, whereas the vertical sections can act as isolation regions.

In this paper, a novel technology is presented which can be applied to fabricate ultra high density memory arrays.

2. TEST STRUCTURES

In order to evaluate the technology 4 x 8 bit NAND-type [1] test ROMs were used. The circuit diagram, the layout of the array and a 3D-view can be seen in Fig. 1a to 1c, respectively.

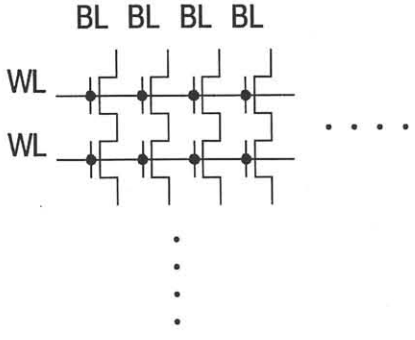

Fig. 1a. Equivalent circuit of the cell array. (WL: wordline, BL: bitline as in ROMs).

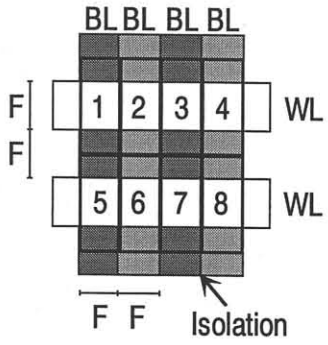

Fig. 1b. Part of layout of the array shown in Fig. 1a with planar MOS transistors and vertical isolation. F: Minimum structure size.

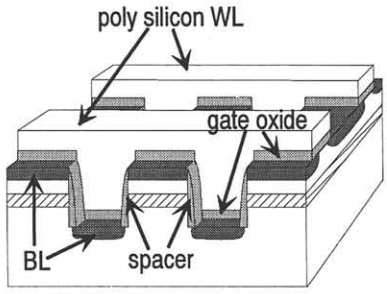

Fig. 1c. 3D-view of the same array as in Fig. 1b.

The semiconductor surface is folded by etching long trenches, so that alternating planar regions at the bottom and between trenches and vertical regions at the side-walls are generated. This doubles the usable device area compared to a conventional planar array (Fig. 1d).

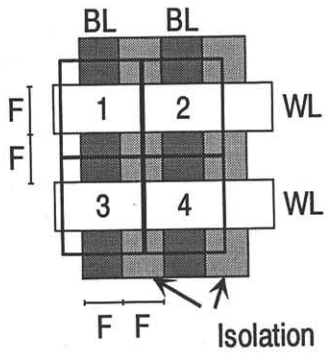

Fig. 1d. Top view of a 2 x 2 ROM cell array with four planar MOS transistors and planar isolation consuming the same area as the 4 x 2 array in Fig. 1b.

The minimum effective area consumption is reduced from $4F^2$ to $2F^2$, where F denotes the minimum structure size. Fig. 1c shows that the devices are grouped on two levels:

1. between trenches and
2. at the bottom of trenches.

Strings of planar memory cells are placed at the bottom of trenches and on top of the Silicon surface between two trenches. They consist of enhancement type MOS transistors and highly As-implanted channel regions representing the physical states "0" and "1", respectively. The bottom and top transistors are isolated from each other by the trench side-walls that act as vertical isolation regions similarly to a one-sided box-type isolation. Thus, this vertical isolation region does not consume any cell area.

The basic processing steps for the test array are trench etching and fabrication of the planar MOS transistors. The trench depth can be chosen equal to the depth of a shallow trench isolation ensuring compatibility to advanced CMOS technologies. The test array MOS transistors are the same devices as NMOS transistors of CMOS peripheral circuits. They are processed simultaneously with them.

The polysilicon layer for the gates is isolated from the trench side-walls by oxide spacers. The polysilicon is etched highly selectively to SiO_2 for structuring the polysilicon across the test cell array. To rule out unintended doping of the side-walls by the channel and source/drain ion implantations, a 0°-ion beam is used.

Figs. 2 and 3 show SEM pictures of the memory cells.

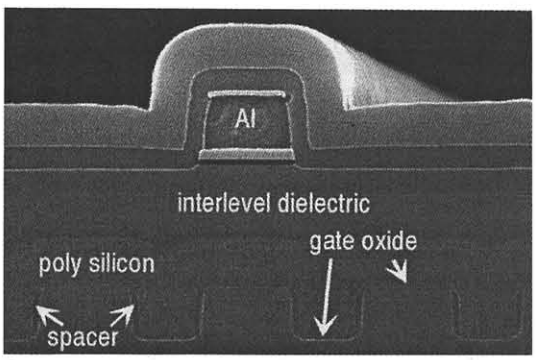

Fig. 2. SEM cross section of a fully processed memory cell array.

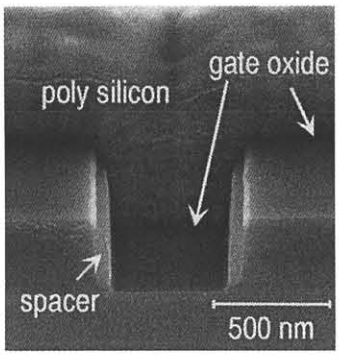

Fig. 3. SEM picture of memory cell MOS transistors at the semiconductor surface between trenches and at the bottom of the trench.

3. EXPERIMENTAL RESULTS

Top and bottom MOS transistors show a turn-off behavior and I-V characteristics (Fig. 4a, b) that are equal to standard planar MOS transistors, i.e., there are no parasitic effects due to the isolating trench side-walls which border the top as well as the bottom MOS transistors. Trench bound devices known from STI-technology [2] are similar to our top devices. However, the trenches are filled with oxide after device fabrication in our case. Furthermore, we showed for the first time the feasibility of a novel trench side-wall bound MOS transistor.

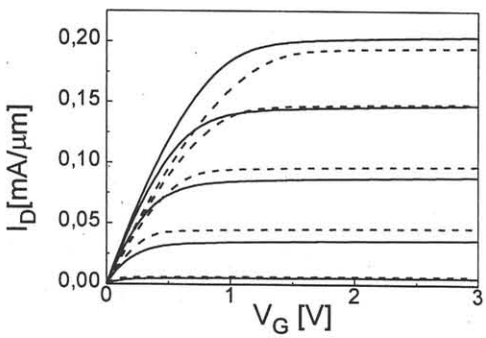

Fig. 4a. I-V characteristics of top (solid lines) and bottom MOS transistors (dashed lines).
(L_{pol} = 0.6 µm; t_{ox} = 10 nm; V_G from 0.5 V to 2.5 V).

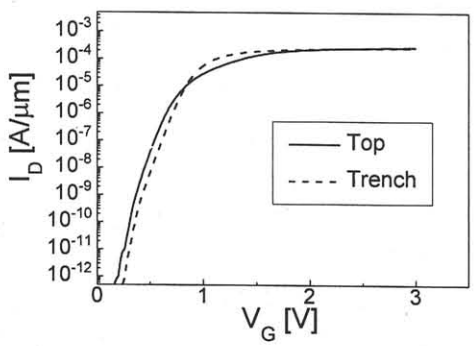

Fig. 4b. Turn-on behavior of top and bottom MOS transistors (same as in Fig. 4a.);V_D = 100 mV.

The polysilicon layer forms together with the trench top and bottom regions a parasitic vertical MOS transistor. Its threshold voltage can be controlled by the thickness of the trench side-wall spacers and a boron layer positioned at about half of the trench height (s. inset of Fig. 5). Fig. 5 shows the increase of the threshold voltage as a function of the implantation dose of the boron.

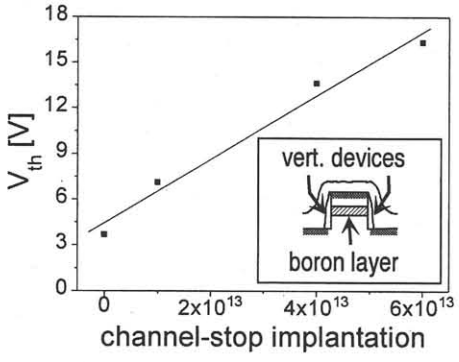

Fig. 5. Threshold voltage of parasitic vertical MOS transistor versus dose of channel-stop implantation (boron layer).

Fig. 6 illustrates the I-V characteristics of the parasitic vertical MOS transistor. Increasing the dose of the channel stop implantation only moderately affects the punch-through voltage between top and bottom MOS transistors, as Fig. 7 shows. The depth of the trenches was 550 nm.

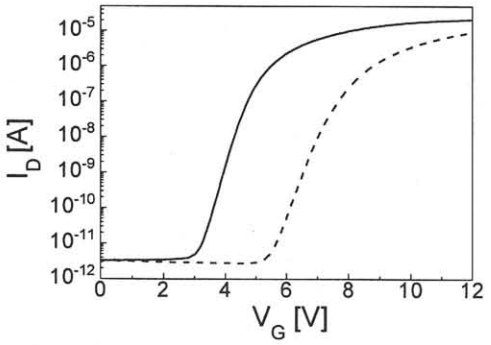

Fig. 6. Turn-on behavior of parasitic vertical MOS transistors without channel-stop implantation (solid line) and with a dose of 1e13 cm^{-2} (dashed line).

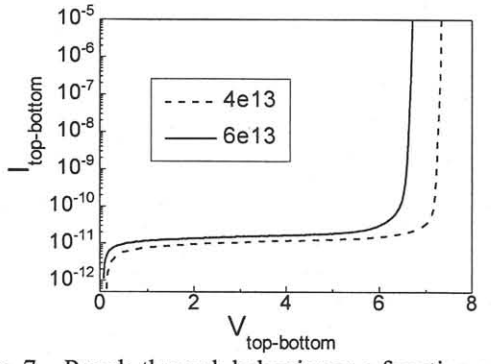

Fig. 7. Punch-through behavior as a function of the drain voltage difference between top and bottom MOS transistors. Parameter is the dose of the channel-stop implantation.

The 4 x 8 bit cell array was fabricated in a 0.6 µm CMOS production line. For read operation, V_{DD} is applied at all but one wordline. This wordline, the row address, is connected to ground. In case of an enhancement MOS transistor, no current flow can occur at the bitlines, whereas for a highly As-implanted channel region signal current flows. A signal current ratio up to 10^6:1 was achieved for reading a "1" and a "0" (Fig. 8).

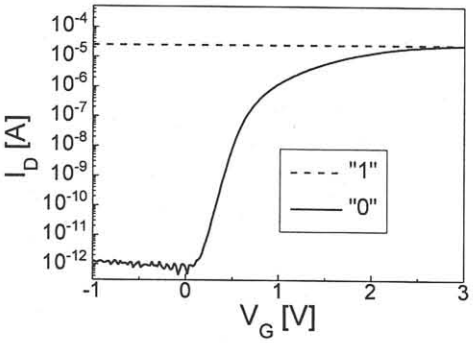

Fig. 8. Signal currents in case of reading a physical "1" and "0" for a string of eight memory cells.

This ratio allows very long NAND-chains supporting an area-efficient design of the cell arrays and peripheral circuitry. Using vertical active MOS transistors, cell arrays in NOR-configuration can be realized [3].

4. CONCLUSION

We demonstrated that MOS transistors at the bottom of trenches and on top of the Si-surface between shallow trenches can be produced and show excellent performance. Parasitic devices between top and bottom can be effectively suppressed. This novel technology allows the fabrication of ultra high density MOS device arrays for Gigabit memory applications.

5. ACKNOWLEDGMENT

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6. REFERENCES

[1] H. Kawagoe and N. Tsuji, IEEE J. Solid-State Circ. SC-11 (1976) 360.
[2] B. Davari, C. Koburger, T. Furukawa, Y. Taur, W. Noble, A. Megdanis, J. Warnock, J. Mauer, IEDM Techn. Dig. (1988) 92.
[3] E. Bertagnolli, F. Hofmann, J. Willer, R. Maly, F. Lau, P.W. von Basse, M. Bollu, R. Thewes, U. Kollmer, U. Zimmermann, M. Hain, W.H. Krautschneider, A. Rusch, B. Hasler, A. Kohlhase, H. Klose, to be publ. in Dig. Techn. Pap. Symp. VLSI Techn., 1996.