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Shallow Trench Isolation for Enhancement of Data Retention Times in giga bit DRAM

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In-depth comparison between STI and LOCOS for DRAM product application is firstly evaluated. The most advanced LOCOS can not meet isolation requirement below 0.25μm design rule. However, STI can meet the isolation characteristics even below 0.20μm design rule. Furthermore, the junction leakage and junction capacitance in STI are reduced, which results in improving sensing signal margin in DRAMs. The main cause of this improvement is found to be relaxed electric field across the junction. This relaxed maximum electric field can also improve the data retention times of STI based DRAMs. The more benefical features of STI are that STI has a wider process window for realizing long data retention times. The improvement of data retention was achieved by optimizing trench depth and LIF implantation in retrograed well process.

1. Introduction

Since STI(Shallow Trench Isolation) was focused as a main isolation scheme for giga bit era, a great efforts have been made in order to realize dishing free and hump free isolation. Recent considerable progresses on STI due to dedicated efforts[1~4] can meet the basic physical (flat surface, no dishing, no oxide dipping in field oxide) and electrical (hump free subthreshold conduction) requirements of giga bit isolation . In spite of a great progress of STI, the adaptation of STI in real product application is very limited in stack based DRAMs due to it's complicated process and the unknown characteristics on data retention time. It is well known that field oxide profile and punchthru stopping field implantation greatly affect the data retention times of DRAMs having LOCOS isolation. In LOCOS based DRAMs, as the device dimension is shrunk, the more field implantation dose is required and the shorter data retention times has been resulted. Below 0.20μm isolation dimension, it seems to be very difficult to have long data retention times. Thus, it is necessary to investigate the data retention times of STI based DRAM having below 0.20μm isolation space. In this study, for the first time to our best knoweldge, in-depth comparison between LOCOS based DRAM and STI based DRAM having 1Gb design rule is firstly evaluated in terms of basic device features. The optimum trench depth and optimized doping profiles related with STI(e.g, channel doping profile of cell transistor) for giga bit DRAMs will be analysed.

2. Experiments and Discussions

The basic key parameters to control isolation are dimension of isolation space, field oxide thickness underneath silicon surface and substrate doping surrounding field oxide. These parameters mainly determine the isolation breakdown voltage, junction leakage current, junction capacitance and subthreshold current of transistor. The isolation length and field oxide thickness and or nitride thickness and so on. In the contrast, these pameters in STI are totally independent and can be separately optimized. In LOCOS, narrow isolation space requires high punchthru-stop field doping to prevent punchthru limited breakdown voltage.

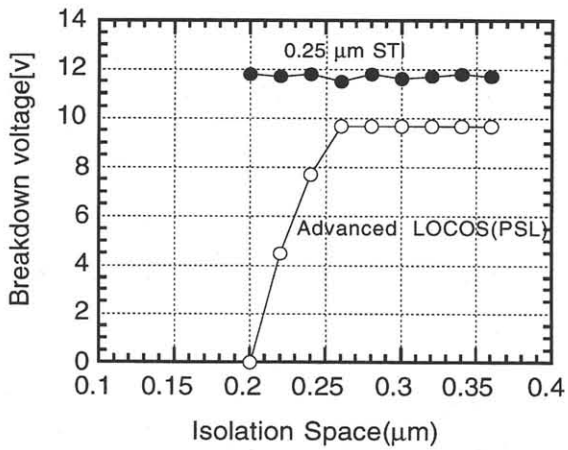

Fig.1 Isolation breakdown voltage vs. STI & LOCOS.

As seen in Fig.1, it is very difficult to realize LOCOS below 0.25μm isolation dimension even if advanced modified LOCOS is used. However, this limitation can be easily resolved in case of STI(see Fig.1). As a result, high electric field is built across the junction, which induces high junction capacitance and high junction leakage as shown in Fig.2 and Fig.3, respectively. However, in STI the electric field across junction can be reduced due to the increase of isolation punchthru length by simply increase of trench depth. The electric field in STI can be lowered as much as factor of three compared to that in LOCOS under same punchthru voltage by accurate device simulatiuon. Hence, considerable improvement of junction capacitance and junction leakage are achieved. The reduced junction capacitance is a great benefit to improve sensing signal margin of memoty cell as shown in Fig.4.

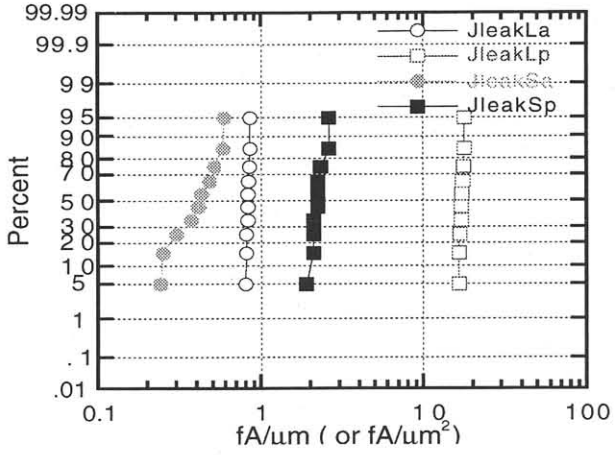

Fig.2 Junction leakage currents vs. STI and LOCOS

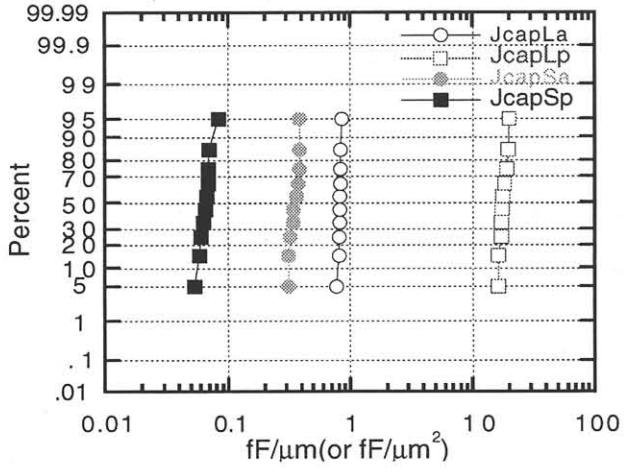

Fig.3 Junction capacitances vs. STI and LOCOS

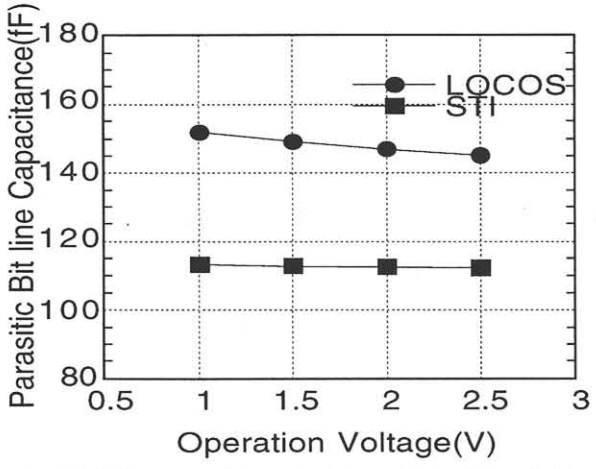

Fig.4 Bit line capacitances(Cb) vs. STI and LOCOS as function of operation voltage(256bits/bit line)

To directly verify how these improvement affect data retention times of real product, an experimental 16M DRAM having giga bit design rules has been fabricated with various trench depth and various doping structures. The key process sequences of STI in this experimental 16M DRAM are shown in the Fig.5. The retrograded twin well process, STI, WSi2 gate, WSi2 bit line, sylinder type capacitor and triple metalliozation process are used in this experimental 16M DRAMs.

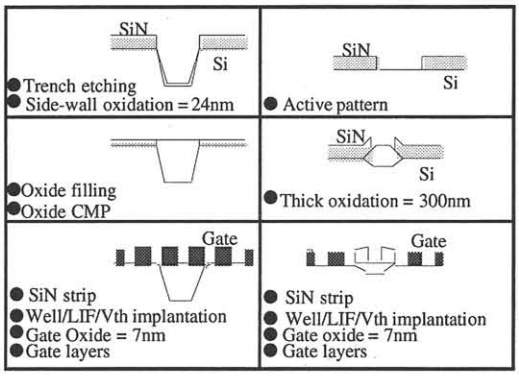

Fig.5 A simplified STI process schematics used in this work

The cross sectional SEM image of cell structure is shown in Fig.6-a. For the careful study on data retention times, well proven NO dielectric capacitor is used. To find the optimum trench depth and LIF(local ion implantation after field oxide) doping structure, the various LIF conditions are investigated with different trench depth as shown in Fig.6-b~d. The effect of diffrent depth of trench on basic device characteristics are summarized as follows: The isolation breakdown voltage, junction leakage current are not much diffrent with variation of trench depth eventhough the periphery junction capacitance is sligtly increased as trench depth is reduced. Therefore, the optimum trench depth for the 0.20μm cell isolation should be determined by characteristics of data retention times.

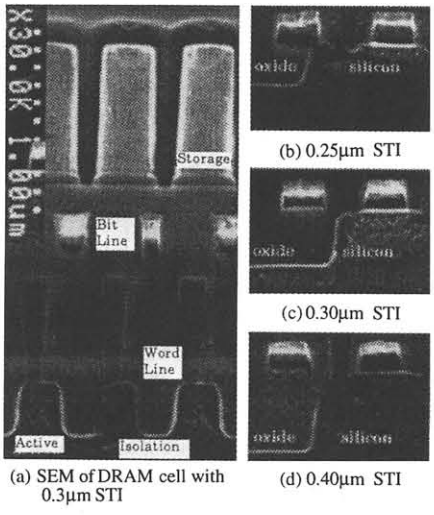

Fig.6 Cross sectional SEM images of cell structure and STI profiles having 0.25/0.3/0.4μm trench depth

As seen in Fig.7, the data retention times are very much dependent on the trench depth and LIF implantation. As trench depth is reduced, the data retention times are decreased. As LIF implantation energy is reduced, data retention times is also reduced. This data imply that the electric field across the cell node junction determine the data retention times due to high electric induced leakage current. The electric field simulation also clearly shows that maximum electric field decreases as trench depth decrease and LIF implantation energy decreases as shown in Fig.8.

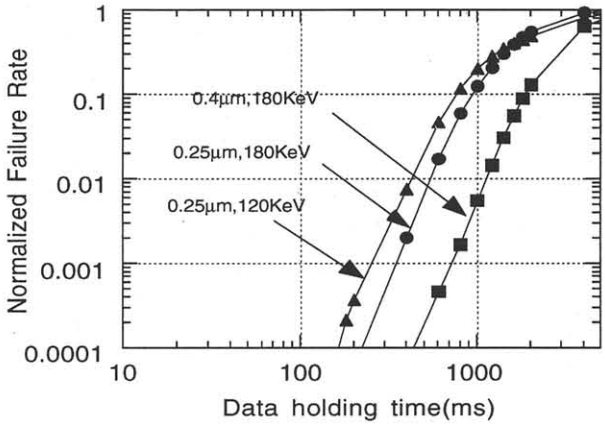

Fig.7 Data retention times vs different trench depth and doping structures of STI in stack DRAM

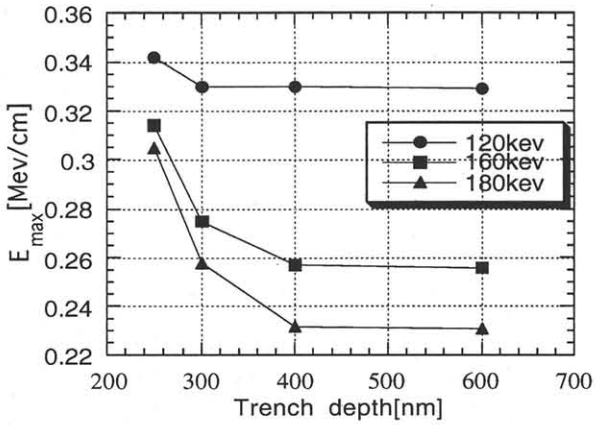

Fig.8 Maximum junction electric field of cell storage node as various trench depth and doping structures.

This kind of high electric field effect on data retention times is well known in LOCOS. It may be concluded that the same mechanism governs the data retention times regardless of LOCOS and STI. However, it should be noticed that the STI has a wider process window for long data retention times. In other words, for example, to increase the data retention times, a deep trench and deep LIF implantation is recommended. This effect will be discussed more in detail in extended abstracr.

3. Conclusion

A better isolation breakdown voltage, junction capacitance, junction leakage current can be achieved in STI compared to LOCOS. The data retention times stroingly imposes the proper trench depth and it's related doping structures of STI. Due to nature of STI, a better process margin can be realized for long data retention times.

4. References

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