Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 836-838

High Performance Shallow Trench Isolation for High Density Flash Memory Cells

S.Deleonibus, M.Heitzmann, Y.Gobil, F.Martin, O.Demolliens, B.Guillaumot(*), P.Candelier and J.C. Guibert.
LETI(CEA); (*)SGS-THOMSON Département de Microélectronique
CENG 17, Avenue des Martyrs 38059 Grenoble Cedex 09 France

Abstract
We combine a LArge Tilt Implanted-Sloped Trench Isolation(LATI-STI) for NMOS and Diffusion Doped Trench Sidewalls for PMOS devices to achieve 0.70µm pitch isolation. High performance periphery devices and high endurance Flash Memories cells of the 64Mbit generation are reported. The trench refill oxide thickness uniformity and dishing after planarization are dependent on die mapping and the mask filling factor mainly. Subthreshold hump suppression under large body bias requires 70° sloped trenches combined with a 50° tilted Boron sidewall implant on NMOS, a diffused N-Well for PMOS. 0.40µm finished N, P metal gate field devices demonstrate higher than 15V isolation.

1.Process flow. Thickness Uniformities.

Figure 1 shows the process flow for the trench isolation steps. 500nm deep, 70° sloped trenches are defined. The steps of active area patterning, sidewall oxidation, N field implant, refill oxide process have already been reported[1]. An Oxide Groove(O.G.) step helps to reduce the thickness uniformity and the so called "dishing effect" i.e. the trench size dependence of remaining field oxide after Chemical-Mechanical Polishing(CMP). Figures 2 show the SEM cross sections after the steps of O.G.(a) or CMP in a 0.7µm pitch array(b) and a semi-infinite trench(c). N+ poly gate buried channel PMOS transistors are optimized in a diffused N-Well. Figures 3 show the different dies mappings compared for die printing. The thickness uniformity and the dishing effect are improved(figures 4a&4b) by combining a suitable die mapping, a high mask filling factor - i.e. the ratio between the masked area and the total die area- and the O.G.'s due to the reduction of the final oxide thickness to be polished.

2.Gate Oxide Qbd.

Minimizing the thermal budget and lateral stress on the trench upper corners after trench etching is important to achieve high QBD 7nm gate oxide(figure 5). The use of O.G.'s allows lower CMP time and a limited oxidation by shadowing of the trench upper corner as compared to the single CMP process (figures 6). A high temperature (1050°C) sidewall oxidation is performed to ensure rounded trench corners. Minimum pre-oxidation deglaze and refill oxide densification times[1] are used to reduce active mask undercut and consequent tipping of the upper corners.

3.Active devices optimization

The differential body effect method- comparison of the quantities ΔVgs and ΔVgw(figure 7a)- is used as a statistical tool to analyze subthreshold behaviour[1] more reliably than the monitoring by subthreshold slope value. Only the W/L=10µm/10µm devices will evidence subthreshold hump(figures 7a&8a) because minimum geometries devices subthreshold characteristics are dominated by short channel effect[1,2]. In the first case, the channel transistor VT is high enough compared to the corner channel transistor VT. Also, reversed narrow channel effects can be analyzed more reliably than in the VT(W) method by using the differential body effect method (figures 7b & 8b). A 70° sloped trench will ease the reduction of subthreshold hump on NMOS[1] (figures 7) or suppress it on PMOS(figures 8) as compared to the 90° slope case. Only the 50° tilted Boron implant on 70° sloped trenches (LATI-STI) suppresses the subthreshold hump on NMOS devices for VB=-10V -(figure 7a) and reference 1)- and reduces the difference between ΔVgs and ΔVgw (the example of narrow channel devices is given in figure 7b). The active corner doping is more easily achieved by using tilted sidewall implant compared to a retrograde (RETRO) implant. The Phosphorous pile-up at the edge of the PMOS active area(figures 8a&b) will reduce the buried channel extension in the bulk of 70° sloped trenches as compared to the 90° case. Consequently, the clamping of the active devices sidewall leakage will be eased.

4.Field devices isolation and junction leakage

0.40µm N and P metal gate field devices punch-through is lower than 10pA/µm at 15V (figures 9a&b). A plugging effect of the refill oxide due to CMP dishing is observed on N channel field devices: the drain depth at the edge of active area is reduced by the thicker oxide shadowing and the isolation of 0.40µm field devices is improved compared to 1.2µm devices(figure 9a). Due to the Phosphorous pile-up at the p+/N-Well junction, a classical behaviour is obtained on P field devices(figure 9b): the -16V avalanche breakdown voltage will limit the 0.40µm and 1.2µm metal gate field devices isolation (@10pA/µm leakage).

5.High performance 0.30µm/0.35µm Flash Memory cells are achieved with reading current of 85µA , ΔVT=4V achieved in 10µs after writing ,6.5% transconductance variation associated to band to band tunneling on the source side together with a programming window degraded by 1.5V after 10^5 write-erase cycles[3] (figure10). The results are identical to those obtained by using a High Temperature Poly Buffer LOCOS reference previously optimized[4, 5].

Acknowledgements Work achieved in the frame of the SGS THOMSON/LETI Joint Program on Flash Memories. The LETI/ST personnel of the Microelectronics Department performed the process and testing of the devices.

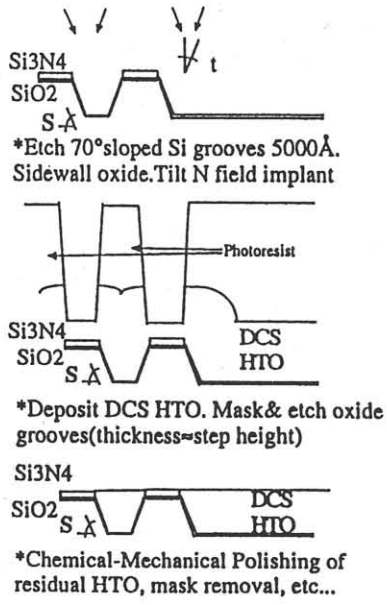


Figure 1 Process sequence after N-Well diffusion

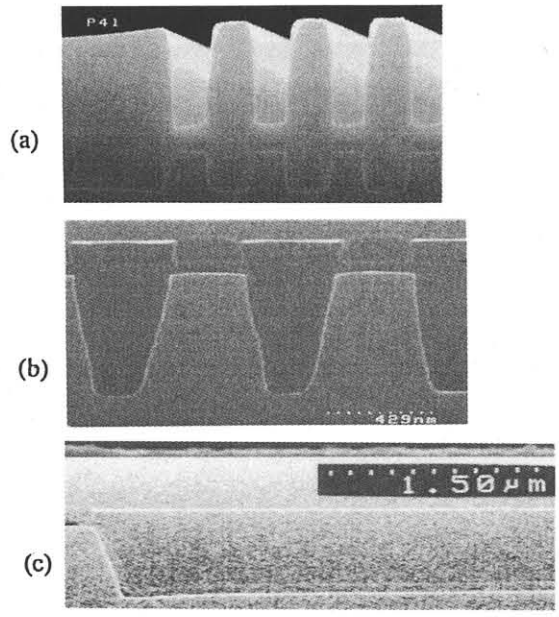


Figure 2 SEM cross sections after:
(a) Oxide Grooves(O.G.) etch
(b) CMP 0.7µm pitch array
(c) CMP semi-infinite spacing

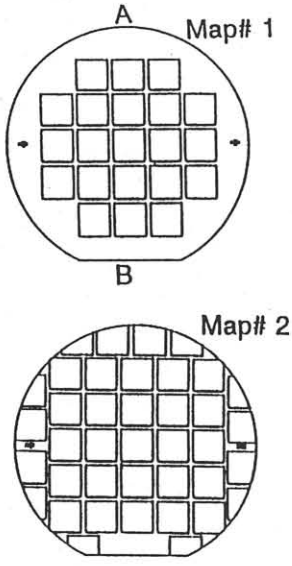


Figure 3 Compared dies mappings

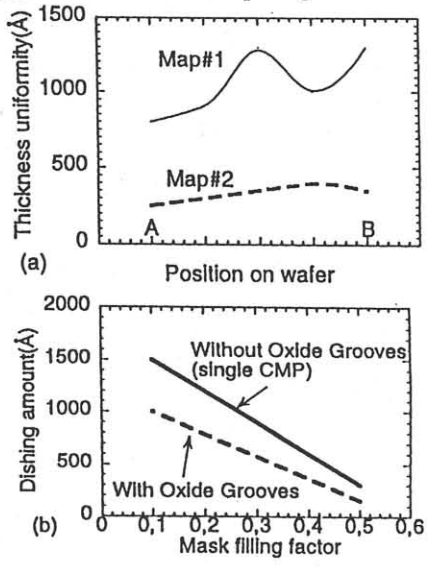


Figure 4 Thickness uniformity
(a) accross 10 wafers diameter
(b) dishing effect 500µm distant isolated points.

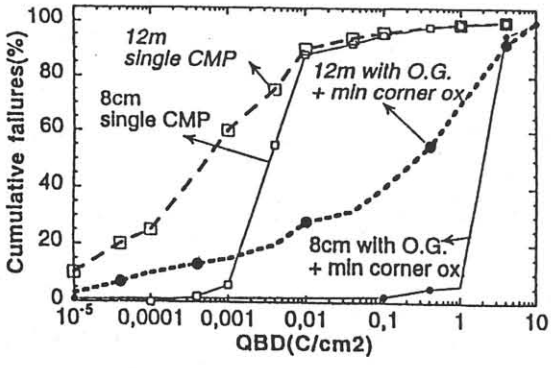
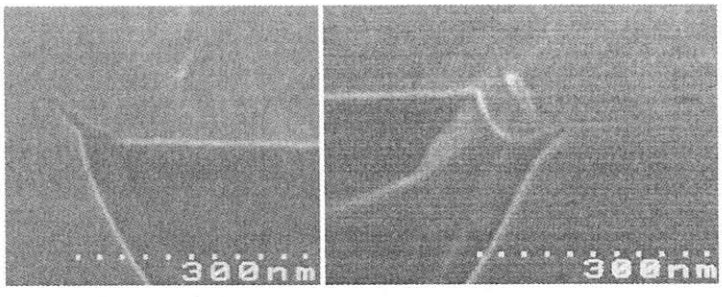


Figure 5 Cumulative failures of small and large perimeter active areas capacitors QBD. Sampling: 210 capacitors/split



(a) (b)

Figure 6 SEM cross sections of active edge for:
(a) Single CMP process (b) O.G. process and minimized corner oxidation process.

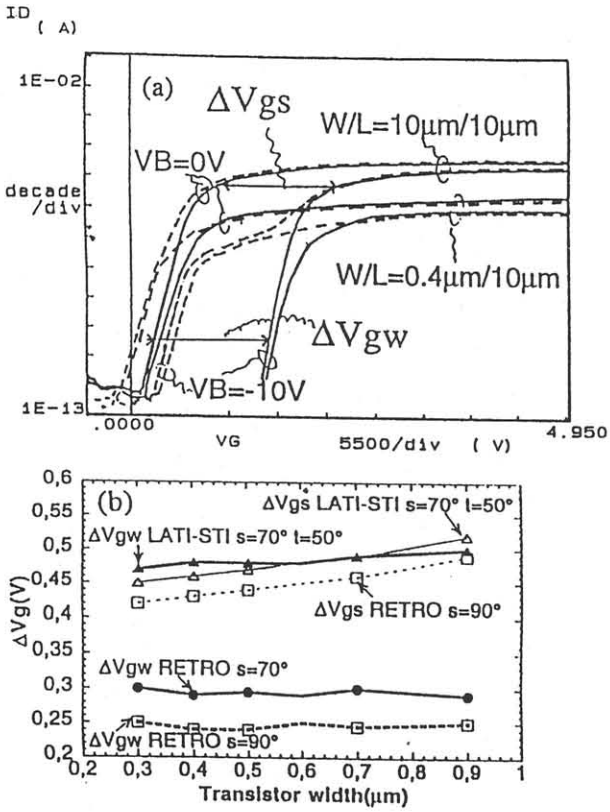


Figure 7 NMOS devices (a) Subthreshold Id(Vg) characteristics.Solid: Boron LATI-STI s=70°; t=50°. Dashed: RETRO s=90°. (b) ΔVg(VB=-3V) as a function of transistor width.

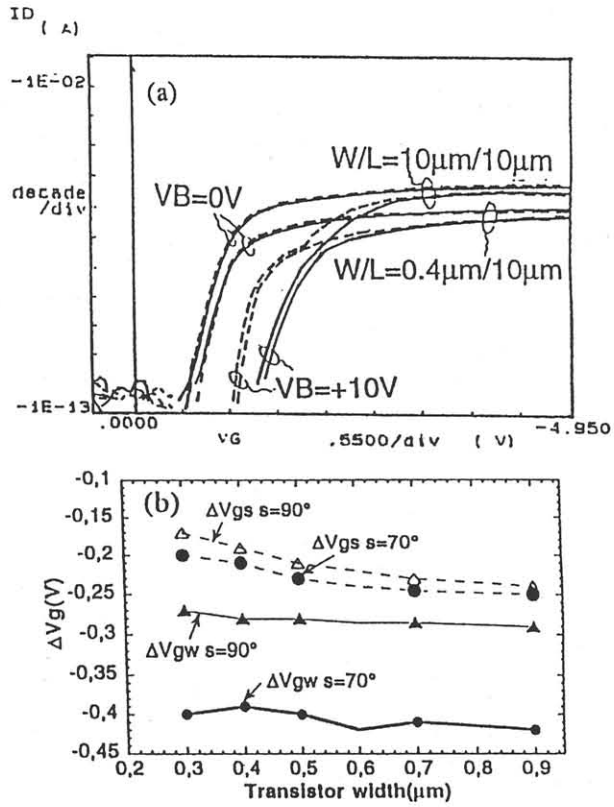


Figure 8 PMOS devices (a) Subthreshold Id(Vg) characteristics.Solid: s=70°. Dashed: s=90°. (b) ΔVg(VB=+3V) as a function of transistor width.

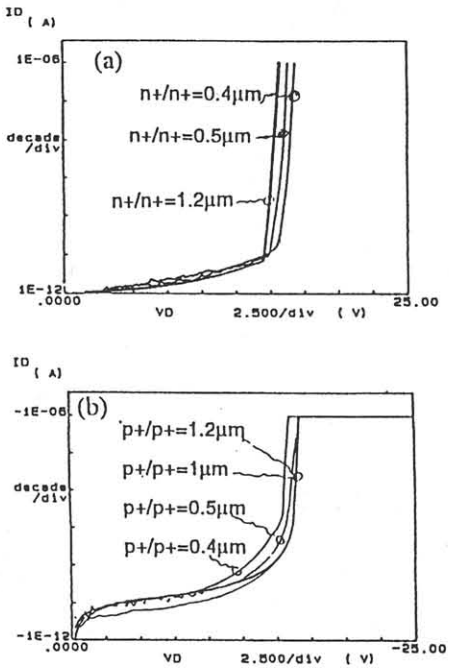


Figure 9 2000μm wide Metal gate field devices punch-through characteristics (a) N field Boron LATI-STI s=70°; t=50° (b) P field s=70°.

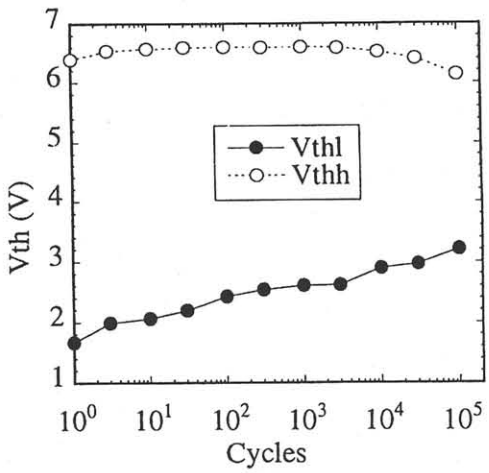


Figure 10 Cell endurance test. 1 cell write among 16k. Vthl: after 10μs write stress. Vthh: after erase. (Write:Vcg=+10V,Vds=+5V; Erase:Vcg=-13V,Vs=+4.5V)

References

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2) A.Bryant et al. IEDM 1994 Proc., pp.61-64, Dec. 1994, Washington(D.C.).
3) B.Guillaumot et al., Presented at INVMTC'96, Albuquerque(NM), June 1996
4) S.Deleonibus et al. SSDM 1994 Proc. pp.913-915, Aug 1994, Yokohama(Japan)
5) B.Guillaumot et al, Non Volatile Memory Workshop 1995