Non-Volatile Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FETs Using PLZT/STO/Si(100) Structures

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We report fabrication and characterization of p-channel metal-ferroelectric-insulator-semiconductor (MFIS)-FETs using the PLZT/STO/Si(100) structures and demonstrate nonvolatile memory operations of the MFIS-FETs. It is found that $I_D$-$V_D$ characteristics of PLZT/STO/Si MFIS-FETs show a hysteresis loop due to the ferroelectric nature of the PLZT film. It is also demonstrated that the $I_D$ can be controlled by the "write" pulse, which was applied before the measurements, even at the same "read" gate voltage.

1. INTRODUCTION

Recently, there has been a growing interest on ferroelectric materials for non-volatile memory applications. Non-volatile memories using ferroelectric capacitors have been widely studied, which utilize basically destructive read operations. On the other hand, nonvolatile memories using metal-ferroelectric-semiconductor field-effect transistors (MFSFETs)\(^1\) make non-destructive read operation possible. In addition, MFSFETs can be used as adaptive-learning analog memories in neural network systems\(^2\). However, preparation of the ferroelectric/Si structures with good interface is not an easy task because of the chemical reaction of Si and ferroelectric materials. Particularly, it is well known that ferroelectric PbZrTiO\(_3\) (PZT) films easily react with Si and inter-diffusion of Pb and Si at the PZT/Si interface occurs even at temperatures as low as 500 °C.\(^3,4\) Nakao et al.\(^5\) reported MFMIS (metal-ferroelectric-metal-insulator-semiconductor) FET structure using PZT and SiO\(_2\) as a ferroelectric film and a gate insulator. In this structure, the excellent interface properties of SiO\(_2\)/Si is available. However, it becomes difficult to apply sufficient voltage to the PZT film because the dielectric constant of PZT films is much higher than that of SiO\(_2\)($\varepsilon_r=3.9$). Consequently, it needs high operation voltage to apply large enough voltage to reverse the polarization of the PZT film.

In this work, to overcome these difficulties, we use a SrTiO\(_3\) (STO) buffer layer to grow the PLZT films on Si substrates. Hence, we refer to the PLZT/STO/Si structure FETs as metal-ferroelectric-insulator-semiconductor (MFIS) FETs. Since the dielectric constant of STO is as large as 300, one can apply the large enough voltage to reverse the polarization of ferroelectric PLZT film. In this paper, we report nonvolatile memory operations of p-channel MFIS-FETs, by using a combination of a high-$\varepsilon_r$ STO buffer layer and a ferroelectric PLZT layer with a relatively low dielectric constant ($\varepsilon_r=240$).

2. SAMPLE PREPARATION

The device structure is illustrated in Fig.1. First, boron-diffused source and drain regions were formed using n-Si(100) substrates. Then, the STO buffer layer and the PLZT (La:6%, Zr:Tl=30/70) film were deposited by the sol-gel method. The annealing conditions were 800°C-30min for STO and 700°C-1min for PLZT films. The typical thicknesses of STO and PLZT films were 70nm and 400nm, respectively. Experimentally measured relative dielectric constant of the STO buffer layers was about 70, because of the presence of 3.3 nm SiO\(_2\) at the STO/Si interface. Hence, to apply the voltage which is large enough to reverse the polarization of the ferroelectric film, a ferroelectric layer with a relatively low dielectric constant is necessary. In this work, we use the PLZT film with a low Zr/Ti ratio (Zr/Ti=30/70) to reduce the dielectric constant. The relative dielectric constant of the PLZT film used in this work is 240. Finally, after contact holes for source and drain were formed by wet chemical etching, the Al electrodes were formed by vacuum evaporation. For comparison, MISFETs with only STO gate insulator was also fabricated. The channel length and width were 40μm and 160μm, respectively.

Fig. 1 Schematic cross section of the PLZT/STO/Si MFIS-FET fabricated in this work.
3. RESULTS AND DISCUSSION

First, we measured the capacitance-voltage (C-V) characteristics of STO (70 nm)/Si structures and observed no hysteresis, indicating that the charge injection or ion drift effects is negligibly small. The interface state density estimated from the C-V characteristics is 6 x 10^10 ev^-1 cm^-2. Figure 2 shows C-V characteristics of the PLZT/STO/Si structure. A counter-clockwise hysteresis loop is clearly seen. Since no hysteresis was observed when only STO is deposited on Si, the hysteresis is believed to be due to the ferroelectric nature of the PLZT film. A memory window (width of the hysteresis loop) is about 0.6 V, which can be used for device applications.

Figure 3 shows I_D (drain current)-V_D (gate voltage) characteristics of STO/Si MISFET without a ferroelectric PLZT layer. It is found that normal MISFET characteristics are obtained, showing no hysteresis, which is consistent with the C-V measurements. I_D (drain current)-V_G (drain voltage) characteristics of STO/Si MISFET are shown in Fig. 4, varying the gate voltage from -4 to -1 V, indicating normal operation of MISFETs.

On the other hand, it is clearly found in Fig. 5 that I_D-V_G characteristics of PLZT/STO/Si MISFETs show a hysteresis loop due to the ferroelectric nature of PLZT films.

A memory window, i.e. threshold voltage shift of the fabricated device was 0.6 V for a V_G sweep from -7 to +3 V. This value also agrees with twice of the coercive voltage (2Vc) of the PLZT film, which suggests the reasonable operation of the MISFETs fabricated in this work. A hole mobility was estimated to be 79 cm²/Vs.

Next, to examine the memory effect of the fabricated PLZT/STO/Si MISFETs, I_D (drain current)-V_G (drain voltage) characteristics were measured by varying "write" and "read" voltages. First, -7 or +2 V "write" voltage was applied to the gate for about 1 s. Then the gate voltage is adjusted at -2 or -3 V ("read" voltage) for the drain current measurements. Figures 6 (a) and (b) show measured I_D-V_D characteristics of PLZT/STO/Si MISFETs. Figure 6 (b) is a re-plot of Fig. 6 (a) in logarithmic scales. Solid and dashed lines show the drain currents after the "write" voltage of -7V and +2 V were applied to the gate, respectively. The "read" gate voltages are 2 or -3 V for both cases. The saturated drain current I_DS is 74 µA when the "write" and "read" voltages are -7 and -3 V, respectively, whereas the I_DS is reduced to as small as 3 µA even at the same gate voltage of -3 V, when the "write" voltage is +2 V. It is
also demonstrated that when the "read" gate voltage is -2V, a transition from "on" to "off" states can be obtained by the previously applied "write" voltage, which is due to the polarization reversal of the ferroelectric PLZT film. The drain current of "on" state (37 μA) is more than three orders of magnitude larger than the "off" state drain current (10 nA) at a V_g=-2V. It is worth noting that the I_D can be significantly changed due to the "write" voltage, which was applied before the measurements, even at the same "read" gate voltage. This clearly demonstrates the memory operation of the PLZT/STO/Si MFIS-FET.

![Graph] Fig. 6 I_D-V_o characteristics of PLZT/STO/Si MFIS-FET. Solid and dashed lines show the drain currents after -7V and +2V "write" voltages were applied to the gate, respectively. The "read" gate voltages are -2 or -3 V for both cases.

Finally, the memory retention characteristics were measured by keeping the gate voltage at -2 V after the "write" voltage (-7 V or +2 V) was applied. Figure 7 shows the drain current as a function of time. The initial value for the drain currents are 37 μA and 10 nA for the "write" voltages of -7 and +2 V, respectively. It is found that the drain current decreases gradually from 37 to 27 μA after 1 h when the "write" voltage was -7 V. On the other hand, when the device is initially at the "off" state, the drain current increased rather rapidly after 30 min (1800 s).

Fig. 7 Time dependence of the drain current of the PLZT/STO/Si MFISFET when the gate voltage is kept at -2 V.

The drain current difference ΔI_DS, which is initially 37 μA, is reduced to 8 μA after 1 h and finally ΔI_DS becomes zero after 2 h. These drain current changes are believed to be due to the depolarization field which has been applied to the ferroelectric PLZT layer throughout the measurements.

4. SUMMARY

MFISFETs using PLZT/STO/Si structures were fabricated and electrical properties of the MFISFETs have been demonstrated. I_D-V_o characteristics of STO/Si MISFETs without a ferroelectric PLZT layer showed no hysteresis, whereas a hysteresis loop due to the ferroelectric nature of PLZT films was clearly observed in I_D-V_o characteristics of PLZT/STO/Si MFIS-FETs. It was also demonstrated that the drain current of the PLZT/STO/Si FETs was controlled by a previously applied "write" pulse. This demonstrates the nonvolatile memory operations of MFISFETs using PLZT/STO/Si structures.

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References