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Effective KOH Etching Prior to Modified Secco Etching for Analyzing Defects in Thin Bonded SOI Wafers

Kiyoshi Mitani, Hiroji Aga, and Masatake Nakano
Isobe R&D Center, Shin-Etsu Handotai Tel: 0273-85-2575
2-13-1 Isobe, Annaka, Gunma, 379-01, Japan Fax: 0273-85-2774

The modified Secco etching method(1), as shown in Fig.1, is effective to detect threading dislocations generated in SIMOX material. Etch pits created by this etching were confirmed to be in agreement with dislocations found by TEM. Recently, it was reported(2) that when this modified Secco etching method was applied to bonded SOI wafers thinner than 1um produced by the Plasma Assisted Chemical Etching (PACE) process(3) including touch polishing, similar etch pits with $10^3 \sim 10^6/cm^2$ in density appeared in these bonded SOIs. Since these etch pits were solely corresponding to threading dislocations in SIMOX material, when the same etch pits were discovered in bonded SOI, these were thought to be related to dislocations. However, there has been no report to confirm the species of defects or to find the origin of defects found in thin bonded SOI wafers. It is essential to verify the discrepancies that the crystal quality of bonded SOI thicker than 1um has been believed to be as good as that of bulk silicon and that more than expected etch pits were found in thin bonded SOI.

Thus, first of all, the existence of these etch pits on 250nm thick bonded SOI wafers thinned through the PACE process was verified. As shown in Fig.2, two types of etch pits were seen. One was pits independent of each other. The other was pits with polishing scratch patterns. Pairs of pits as usually seen in SIMOX were not found. Also, comparing Fig.2(a) and (b), the pit density appeared to be dependent on etching removal depth of SOI layers. The increase of etch pit density vs. remaining SOI thickness after the modified Secco etching was plotted in Fig.3. As shown in the figure, higher density of etch pits was observed when larger volume of SOI surfaces was removed by the etchant. Since this modified Secco etching method counted the number of defects which existed in SOI layers removed by the first diluted Secco etching in the whole modified Secco etching process, the dependence of the pit density on the removal volume of SOI layers indicated that the density of defects detected by this etchant was not constant but had a certain distribution in the SOI thickness direction. However, this etching method did not suggest a position or a distribution of defects.

In order to see the distribution of defects in the SOI thickness direction, the surface of SOI layers was sequentially removed by KOH etching before using the modified Secco etching. As shown in Fig.4, the modified Secco etching detected defects wherever they were located in SOI layers. On the other hand, since our method using KOH allowed us to remove desired thickness of SOI surfaces before the modified Secco etching, the defect distribution could be obtained. 1um and 400nm thick bonded SOI wafers fabricated by the PACE process were prepared. The material of the SOI wafers was CZ <100>, p-type silicon with resistivity higher than 1 ohmcm. The buried oxide thickness was 500nm.

Figure 5 shows the defect density corresponding to the removal depth of SOI surfaces by KOH. This figure indicated three results. 1) Defects were primarily located in front SOI surfaces with a Gaussian distribution. It indicated that these defects were caused by damages due to energy forced at SOI surfaces, such as coming from the PACE etching or from touch polishing. The polishing scratch pattern really suggested that the touch polishing influenced on the defects. The damage depth was thought to be approximately 300nm. 2) In the area deeper than 300nm from the surface, the defect density was linearly decreased. It indicated that these defects were uniformly distributed in the bulk SOI layers, which implied the presence of grow-in crystal defects. 3) At 1um, where the SOI/BOX interface was located, the defect density was not zero but some positive numbers indicating the presence of defects at the interface.

In conclusion, by using KOH etching to remove surface SOI layers prior to the modified Secco etching, the defect distribution was effectively obtained. This distribution indicated the origin of defects. In 100nm PACE-processed bonded SOI layers, three different origins of defects were thought to be mixed together.

References

(1) H. Gassel et al., J. Electrochem. Soc., 140, 1713(1993)
(2) P. Roitman et al., Proc. ECS Int. Symp. of SOI (1994)
(3) P.B. Mumola et al., Proc. ECS 2nd Int. Symp. of Wafer Bonding, PV93-29, 410(1993)

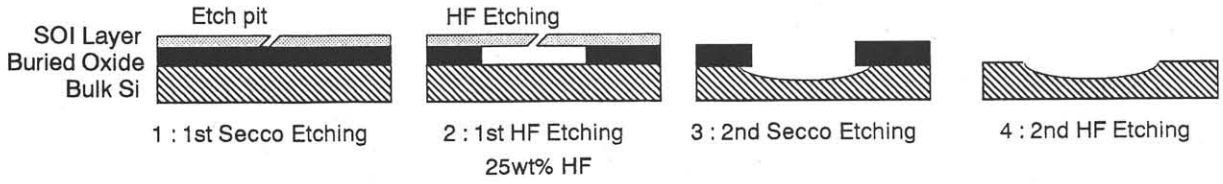

Fig.1 The process flow of the modified Secco etching.

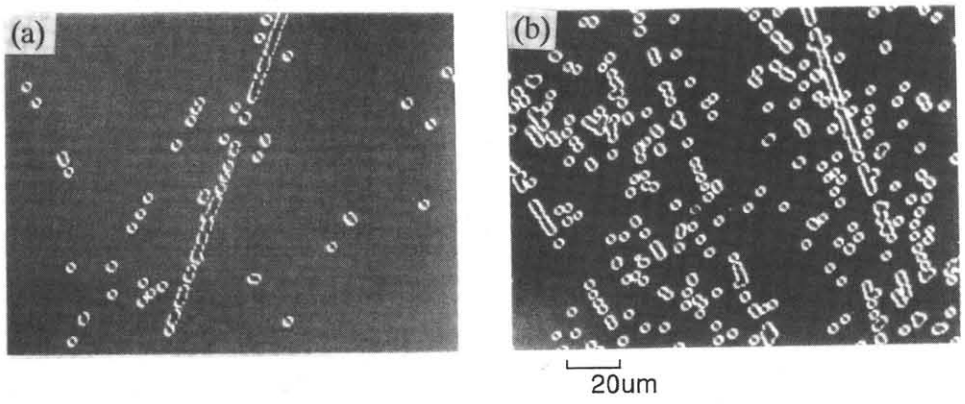

Fig.2 Micrograph of etch pits created by the etching shown in Fig.1. Etch pit density in (a) is lower than in (b). SOI layer thickness after the first Secco etching was 100nm in (a) and 40nm in (b), respectively.

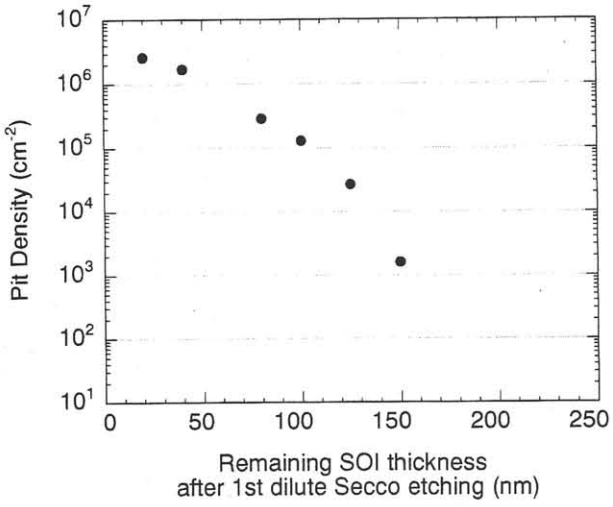

Fig.3 Etch pit density vs. remaining SOI thickness after the first Secco etching.

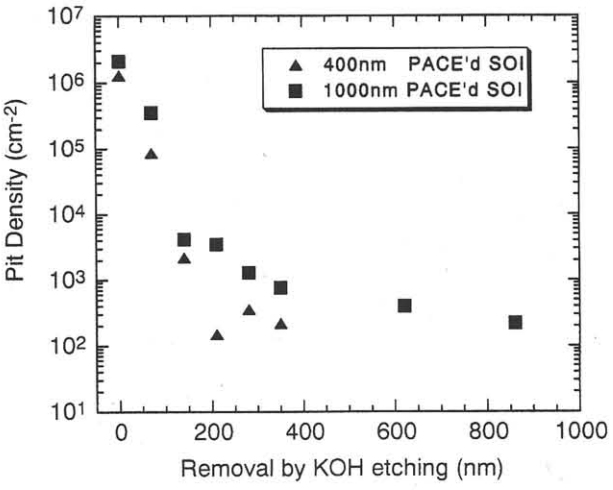

Fig.5 Etch pit density vs. removal thickness of surface SOI layers by KOH.

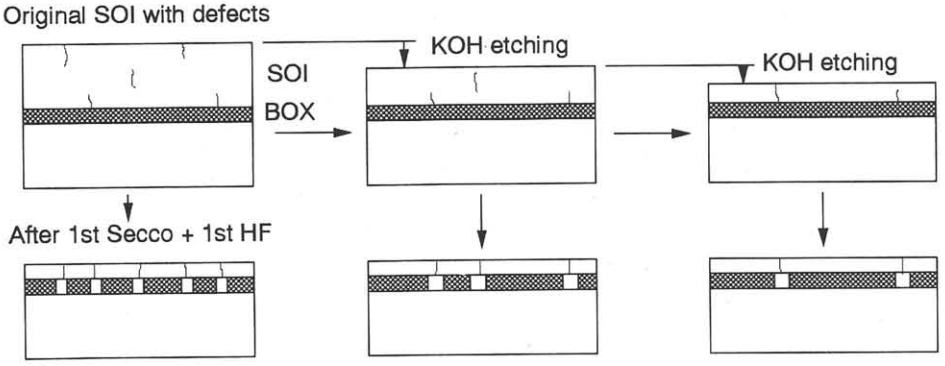

Fig.4 A model of etching steps.