Evaluation of Killer Particle Size in Deep Submicron Devices

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We evaluated killer particle size in deep submicron devices using interconnect layer. Based on our experimental results, we found that killer particle size was the same as or larger than the minimum feature size of device down to 0.35 μ m rule wiring, and about half the feature size for 0.25 μ m rule device. It is because that hard-mask process used in 0.25 μ m device fabrication is more likely to result in failure caused by defects from particles than the PR-mask process in 0.35 μ m rule device.

1. Introduction

As devices become smaller, tighter control is needed about particle size and particle density. According to SIA roadmap, killer particle size is thought to be about one-third the minimum feature size of the device. [1] In deep submicron devices, killer particles are smaller than 0.1 μ m. The impact of these particles on device yield is considerable because the number of deposited particles increases drastically by the effect of Based on the assumption that electrostatic potential. the killer particle size is about one-third the minimum feature size of the device, the drastic increase of the killer particle on wafers will have serious effect on ULSI fabrication after 256Mbit era compared with previous generation. [2] In this case we will need new concept on cleanroom environments or fabrication process such as full auto-mated fabrication line and mini-environment fab system. The experimental evaluation of killer particle size corresponding to different device generations is very important for controlling contamination in ULSI fabrication.

In this paper, we investigate the effect of particles on yield decrease using 0.25-0.75 μ m short and open check patterns in aluminum wiring. We selected the interconnect layer as a typical process that is largely influenced by particles, because wet cleaning is difficult to apply to metal layers and removal of deposited particles is difficult in metallization.

2.Experiment

Figure 1 shows the structures of a short check pattern and an open check pattern. The short check pattern has a comb structure and the open check pattern has a serpent structure with line and space of 0.25-0.75 µm. Each chip area is 6.25 mm². After patterning photo-resist film on sputtered aluminum film, some of the test wafers were exposed to a class1 cleanroom environment for 40 days while the others were kept in a wafer box. About three particles (>0.16 µm) per day were deposited on a 150 mm wafer in this experiment. After dry etching of aluminum films and removing of resist films, the yields of the short and open check patterns were measured to evaluate the effect of particles deposited from the cleanroom environment. Killer particle density was obtained from the yield, and killer particle size was measured by KLA inspection system.

3. Results and discussion

3-1 Results of short and open check pattern yields

Figure 2 shows the obtained yields for the short check pattern for both the PR-mask and hard-mask processes. A yield reduction of about 20% was observed for a design rule decreased to $0.25 \,\mu m$ when the samples were exposed to cleanroom air for 40 days.

On the other hand, a yield reduction of only 2% was

observed for the sample kept in the wafer box for 40 days. There was no yield decrease for the open check pattern. Since deposited particles on aluminum film act as a mask in dry etching process, these particles cause short failure of interconnect layer. This experimental result was as expected and means that the fine aluminum pattern fabricated well.

3-2 Correlation between particle size before etching and corresponding defect size

Figure 3 shows the SEM review of the defect inspected by KLA. This defect was the smallest defect that caused short mode failure in 0.25 μ m rule. We found that the defect size causing short mode failure needed to be about 1.1 times the feature size.

The SEM review in figure 4 shows examples of particle size and corresponding defect size inspected by KLA . In the hard-mask case, the 0.366 μ m particle made the 0.233 μ m pattern defect on the aluminum layer. In the PR-mask case, however the 0.3 μ m particles on the aluminum layer were sometimes removed completely by aluminum etching. This indicates that the hard-mask process more is more likely to result in failures caused by defects from deposited particles on aluminum layer during aluminum etching than the PR-mask process, because the hard-mask process uses thin SiO₂ film corresponding to the aluminum thickness as an etching resist-mask.

Figure 5 shows the correlation between particle size before etching and pattern defect size after etching for SiO_2 Poly-Si, and aluminum layer. Based on these results, the defect size must be about 1.1 times the feature size or more in the short mode failure. The smallest killer particle size was estimated at 1.0-1.2 times the feature size.

3-3 Calculation of total device yield

Using the data shown in figure 2, we estimated total device yield. Figure 6 shows presumed DRAM yield. The yield of short check aluminum pattern is obtained by the formula Y=1-kDA, where Y is the yield, D is deposited particle density, A is chip size and k is probability of device failure. To calculate the total device yield, we used killer particle density per hour

(=kD) in a class 1 cleanroom environment. The value of kD was obtained from the data shown in Figure 2.

In the yield calculation, we have only taken 10% of the total number of process steps and 1-hour exposure to the class1 cleanroom environment into account. [2] Figure 6 shows the theoretical yields for killer particle size that is one-third the smallest feature size (dashed line) and half the smallest feature size (solid line) and the same as the smallest feature size (dotted line). A drastic decrease will be presumed in yield of a 256M DRAM compared with 1:1 theory line by hard-mask process. Although this may be a direct reflection of the etching process change, killer particle / feature size ratio may decrease from 1.0 in 0.35 μ m rule to half or less in 0.25 μ m rule or smaller rules in the future.

4.Conclusion

Based on these experimental results using interconnect layer, killer particle size was found to be the same as or larger than the feature size down to 0.35 μ m rule wiring, but was about half the feature size in 0.25 μ m rule wiring. This is because the hard-mask process is not necessary for 0.35 μ m rule era, but will be necessary for 0.25 μ m rule era or smaller rules in the future.

Acknowledgment

We would like to thank Drs. Osamu Mizuno, Masanori Kikuchi and Kazuko Ikeda for their encouragement and useful discussion. We would also like to thank Toshiro Itani and Tuyosi Yoshii for KrF lithography, and Hidenobu Miyamoto and Hideaki Kawamoto for aluminum etching.

References

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Fig.1. Structure of (a) short check pattern (b) open check pattern , and chip layout



Fig .3. SEM view of smallest defect failure size inspected by KLA



Fig .5. Correlation between particle size and defect size



Fig. 4. SEM view of particle size before etching and defect size after etching, inspected by KLA(in hard-mask and PR-mask case)



Fig .6. Calculated DRAM Yields obtained from data shown in Fig.2