Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 260-262

High Reliability Trench Isolation Technology with Elevated Field Oxide Structure for Sub-Quarter Micron CMOS Devices

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High reliability trench isolation technology with elevated field oxide structure, the Elevated Trench Isolation (ETI), has been proposed. The formation of trench isolation after gate oxidation allows the use of BPSG as trench filling material, which realizes void-free gap filling in the aspect ratio of 3.5. The ETI provides larger process margin for planarization, which is determined by the thickness of the 1st gate electrode. High gate oxide reliability and good subthreshold characteristics were achieved by using the ETI structure.

1. Introduction

As scaling down to sub-quarter micron region, the Shallow Trench Isolation (STI) technology becomes a key issue to realize high packing density VLSIs. Recent works have paid much attention on the surface topography control during CMP or etchback planarization and void-free filling in the narrow gaps [1][2]. However, the electrical characteristics of the MOSFETs with STI structure strongly depend on the corner shape of trench isolation and trench filling dielectric materials. Moreover, there has been little attention on the thin gate oxide reliability for the MOSFETs with STI.

In this paper, we have proposed high reliability trench isolation technology with elevated field oxide structure, the Elevated Trench Isolation (ETI), which realizes void-free gap filling using BPSG reflow. The dependence of the gate oxide reliability on trench edge is clarified, comparing with that of the conventional STI.

2. ETI process

The processing sequence of ETI is shown in Figure 1 (a)-(f). After ion implantation for retrograde twin-wells, channel stop, and Vt adjustment, 7 nm gate oxide is formed. The trench regions were selectively formed after deposition of 300 nm poly-Si layer as the 1st gate electrode. The trench depth was 400nm (Figure 1 (a) and (b)). 50 nm LP-CVD SiO_2 and thick AP-TEOS/O_3 BPSG films were deposited, followed by annealing for 30 minutes at 850°C (Figure 1 (c)). A thin oxide liner was not grown before LP-CVD SiO_2 deposition. After etchback planarization using poly-Si etch-stop layer (Figure 1 (d)), WSi_x layer was deposited as the 2nd gate electrode (Figure 1 (e)). WSi_x and poly-Si were selectively etched using the field and the gate oxide as stopper-layers. Then the WSi_x/poly-Si gate electrode was formed on the active area, and a single WSi_x layer was formed on the field (Figure 1 (f)). This process scheme allows planar topography of gate electrode.

Figure 2 shows SEM image of SRAM cell with the ETI structure. It is confirmed that the field oxide surface is above the active silicon. In this case, the large process margin for planarization is achieved using the 1st gate poly-Si. Also, the WSi_x layer shows planar topography between the field and active area.

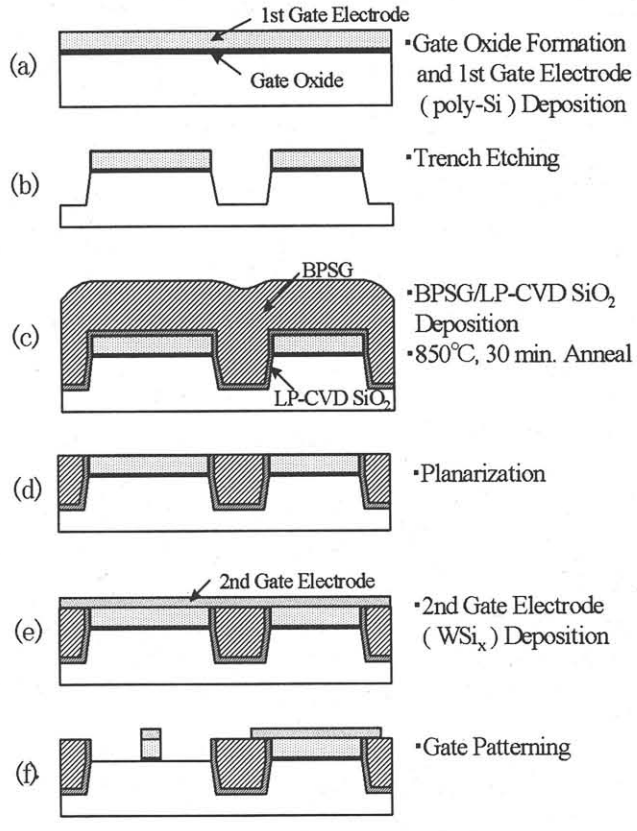


Figure 1. Elevated Trench Isolation (ETI) process flow.

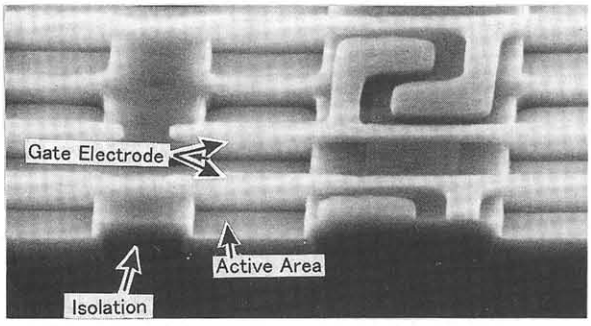
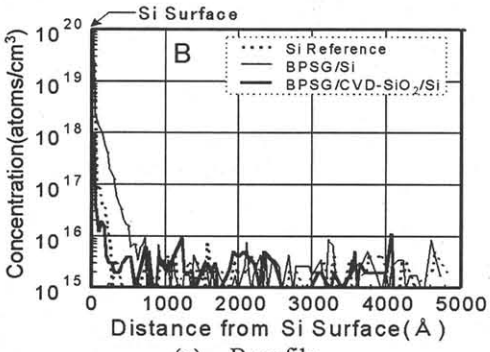
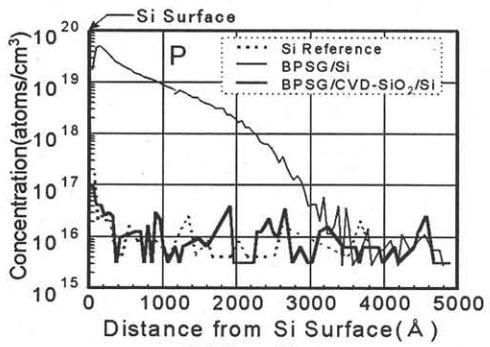


Figure 2. SEM image of SRAM cell after the gate patterning process

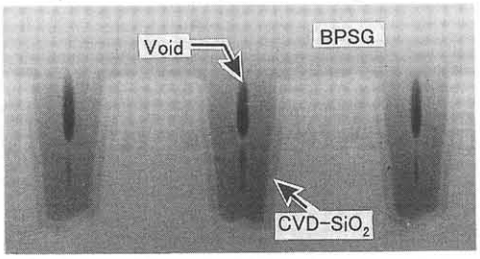


(a) B profile

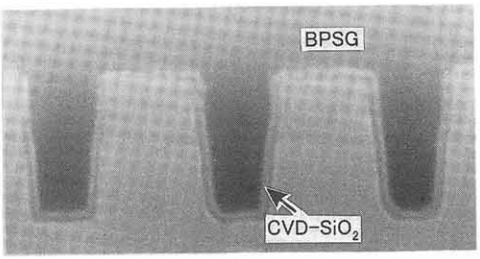


(b) P profile

Figure 3. SIMS profile of (a) B and (b) P in Si substrate after annealing for 60 minutes at 850℃, respectively. CVD-SiO_2 thickness is 50 nm.



(a) as deposited



(b) after annealing

0.4 μm

Figure 4. SEM cross-sectional views of trench filled with BPSG, (a) as deposited (HF:HNO_3 = 1:200, 10 sec. dip-etched) and (b) after 30 minute annealing at 850℃ (HF:H_2O = 1:5, 10 sec. dip-etched).

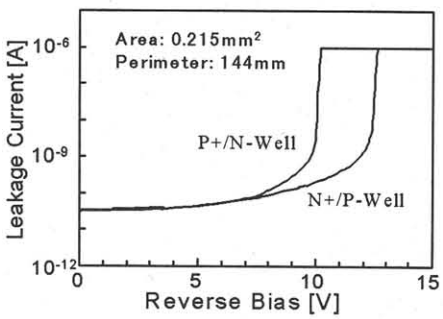


Figure 5. Junction leakage current characteristics for ETI

3. Results and Discussions

3.1 Narrow gap filling

The formation of trench isolation after gate oxidation allows the use of BPSG as trench filling material. Before BPSG deposition, 50 nm LP-CVD SiO_2 film was covered as a stop layer, which prevented from diffusion of both B and P into Si-substrate. The deposition of SiO_2 film is free from size reduction for both active area and poly-Si gate, while the sidewall oxidation reduces the active area and gate pattern. Figure 3 (a) and (b) shows the results of SIMS analysis. It is confirmed that the diffusion of B and P was perfectly suppressed in BPSG/CVD-SiO_2/Si structure, though these atoms diffused into Si substrate in BPSG/Si. Figure 4 (a) and (b) shows gap filling properties at aspect ratio of 2.0, just after BPSG deposition and after heat treatment for 30 minutes at 850℃, respectively. Because of good reflow property of BPSG, void-free gap filling was achieved even though in the aspect ratio of 3.5. Necessity for trench sidewall oxidation to remove silicon RIE damage has been reported [1][3]. However, junction leakage characteristics without soft-breakdown phenomenon, as shown in Figure 5, and good isolation characteristics [4] were obtained without the trench sidewall oxidation.

3.2 Narrow channel characteristics

Figure 6 shows substrate bias voltage dependence of subthreshold characteristics for n-MOSFETs with the ETI structure and the conventional STI structure, which was formed trench isolation before gate oxidation. In the STI structure, the height (H) from Si surface to isolation surface was 50 nm below Si surface. The STI structure (H = -50 nm) induces hump current. In the case of the ETI structure, good subthreshold characteristics without hump current was obtained. This means that in the ETI the corner effect of trench isolation is suppressed. Figure 7

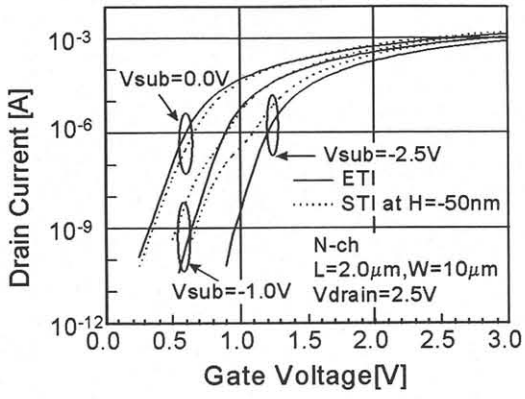


Figure 6. Subthreshold behavior on n-MOSFET.

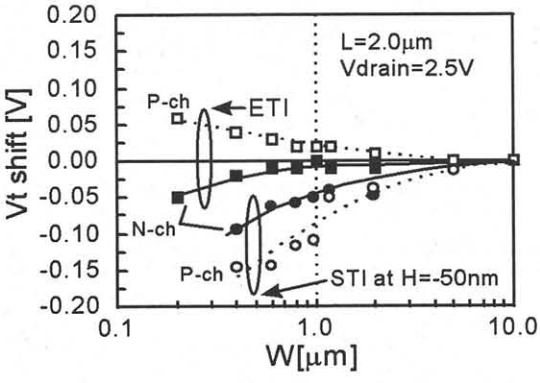


Figure 7. Channel width (W) dependence of Vt shift (|Vt|-|Vt[W=10 μm]|) for n-MOSFET.

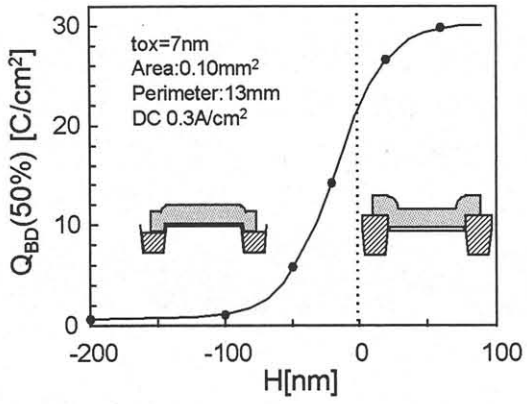


Figure 8. SiO_2 height (H) from active area dependence of Q_{BD} in cumulative failure 50 %.

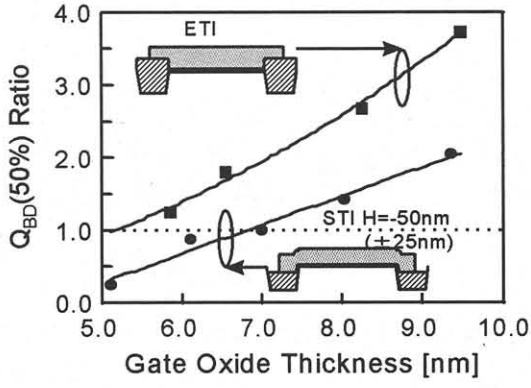


Figure 9. Gate oxide thickness dependence of Q_{BD} in cumulative failure 50 % normalized for Q_{BD} at tox = 7 nm in STI. DC 0.3 A/cm^2 was injected into the gate. The capacitor area is 0.10 mm^2 and the perimeter is 0.13 mm

shows gate width (W) dependence of threshold voltage (Vt). Vt shift was less than 50 mV even at W = 0.2 μm in both n- and p-MOSFETs with the ETI structure, since the isolation surface after planarization is elevated from Si-substrate. It is found that the ETI was effective in suppressing the inverse-narrow channel effect.

3.3 Gate oxide reliability

The high gate oxide reliability of ETI is an important factor to realize shallow trench isolation technology. Figure 8 shows gate oxide reliability (Q_{BD}) of n-MOS gate in cumulative failure 50 % as a function of H in the STI. It is found that high gate oxide reliability is achieved at H > 0 nm, while the Q_{BD} degrades at H < 0 nm. A significant degradation is induced at H < -100 nm. Figure 9 shows gate oxide thickness dependence of Q_{BD} in the ETI and the STI with H = -50 nm. Although the 1st gate poly-Si was used as a etchback-stop layer, the ETI shows twice improvement of Q_{BD} than that of the STI in the wide range of gate oxide thickness. From the luminescence analysis of these samples, it was confirmed that the gate oxide was broken down at the perimeter of active regions in the STI with H < 0nm. Thus high gate oxide reliability is achieved by using the ETI.

4. Conclusions

High reliability trench isolation technology with elevated field oxide structure has been proposed. The formation of trench isolation after gate oxidation allows the use of BPSG as trench filling material, which realizes void-free gap filling. The ETI provides larger process margin for planarization than that of the conventional STI, which is determined by the thickness of the 1st gate electrode. High gate oxide reliability and good subthreshold characteristics were achieved by using the ETI structure.

Acknowledgments

The authors would like to thank Dr. T. Takemoto and Dr. S. Odanaka for their encouragement during this work.

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