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A Novel Dual Gate CMOS Technology Using Low Energy Phosphorous/Boron Implantation and Arsenic Pre-Amorphization

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We have proposed a novel dual gate CMOS technology using low energy phosphorous/boron implantation and arsenic pre-amorphization. By using phosphorous and boron ion and arsenic pre-amorphization, the sheet resistance was reduced and the gate polysilicon depletion was suppressed due to high activation ratio compared with arsenic and BF_2. As a result, higher current drivability for NMOS and PMOS was obtained. This process allows a sub-quarter micron dual-gate CMOS with high current drivability, suppressing both boron penetration and polysilicon depletion effect.

1. Introduction

The development of sub-quarter micron CMOS device requires a dual-gate CMOS process, which allows surface channel PMOS as well as NMOS. The dual-gate process tradeoffs in boron penetration for p^+-polysilicon gate and polysilicon depletion for n^+-polysilicon gate. Much work focuses on suppressing boron penetration and p^+-polysilicon depletion with optimization of annealing time and temperature[1-2]. The purpose of this paper is to present a dual gate CMOS process with high current drivability. It is found that phosphorus implantation decreases polysilicon depletion effect compared with arsenic one in n^+-polysilicon gate and boron implantation combined with arsenic pre-amorphization can suppress both boron penetration and polysilicon depletion in p^+-polysilicon gate.

2. Experimental

The process sequence is shown in Fig.1. After forming field isolation, threshold voltage adjustment was carried out. The thickness of gate oxide and gate polysilicon were 6nm and 200nm, respectively. The gate electrode was patterned by KrF excimer laser lithography. After thin sidewall oxide formation, pre-amorphization implantation (arsenic 60keV,$3x10^{14}cm^{-2}$) was performed, followed by source/drain implantation (phosphorous 10keV, 2-$6x10^{15}cm^{-2}$) for NMOS. The source/drain implantation (boron 10keV, 2-$6x10^{15}cm^{-2}$) for PMOS was performed, followed by rapid thermal annealing at 950-1050 °C.

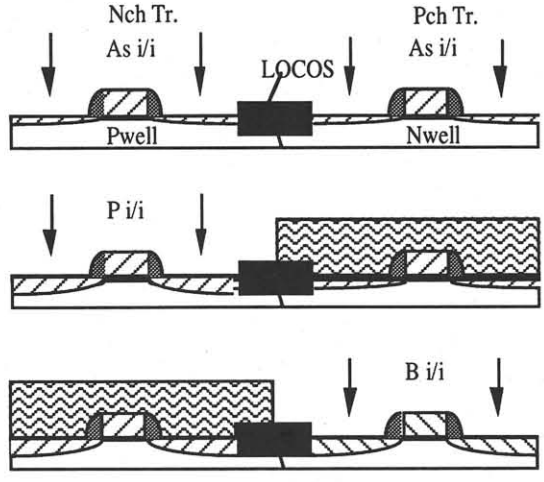

Fig.1 Process sequence of a new dual gate CMOS

3.Results and Discussion

The gate depletion index Cinv/Cox for NMOS is shown in Fig.2. The Cinv/Cox of phosphorous doped gate electrode is higher than that of arsenic one. The Cinv/Cox is 97% for phosphorous doped gate and 93% for arsenic one at a dose of $4x10^{15}cm^{-2}$. The gate depletion index Cinv/Cox for PMOS is shown in Fig.3. The depletion effect of the gate polysilicon of PMOS with boron doped gate was successfully suppressed compared with BF_2 doped gate. The Cinv/Cox for arsenic pre-amorphized boron doped gate reaches 94% at a dose of $4x10^{15}$ cm^{-2}, while the Cinv/Cox for BF_2 doped gate is 90%.

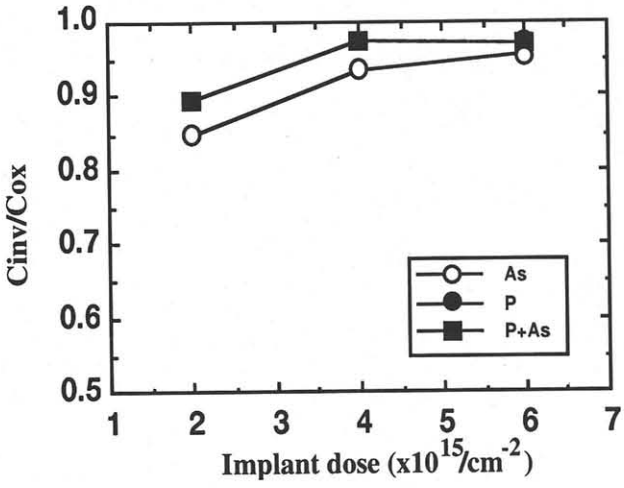

Fig.2 Gate depletion index Cinv/Cox as a function of implant dose for different implant ions.

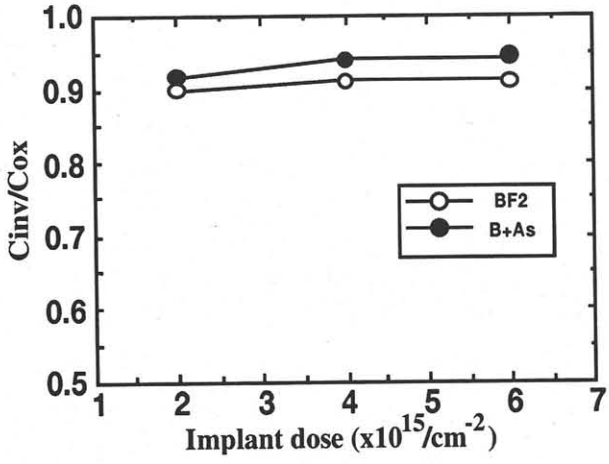

Fig.3 Gate depletion index Cinv/Cox as a function of implant dose for different implant ions.

Fig.4 shows the flatband voltage shift of PMOS as a function of annealing temperature. The flatband voltage shift of polysilicon gate using BF_2 ion is higher than that of boron and arsenic ions. The previous work shows that boron doped gate with Si pre-amorphization suppresses the boron penetration[3]. It is found in this work that the flatband voltage shift for boron doped gate with arsenic pre-amorphization is smaller than that of BF_2 doped one at the same gate implant, indicating that boron penetration can be suppressed by arsenic pre-amorphization and boron implantation.

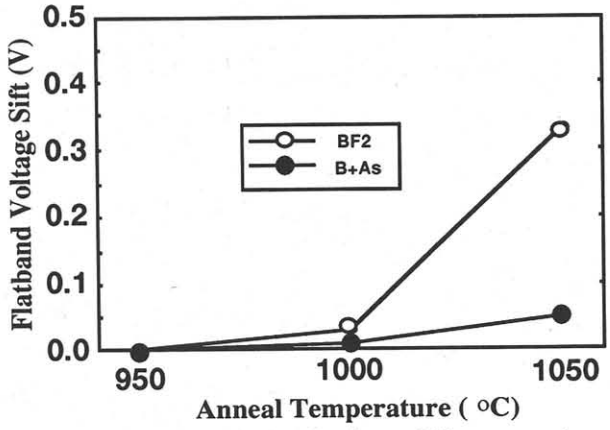

Fig.4 Dependence of flatband voltage shift on anneal temperature for different implant ions.

Fig.5 shows the sheet resistance of polysilicon gate electrode for NMOS. The sheet resistance of polysilicon using phosphorous ion is lower than that of arsenic ions. The sheet resistance of polysilicon for PMOS is shown in Fig.6. The sheet resistance of polysilicon using boron ion is lower than that of BF_2 ion. These results are consistent with depletion index for N and PMOS's, which indicate that the suppression of depletion effect is due to activation of impurity ions.

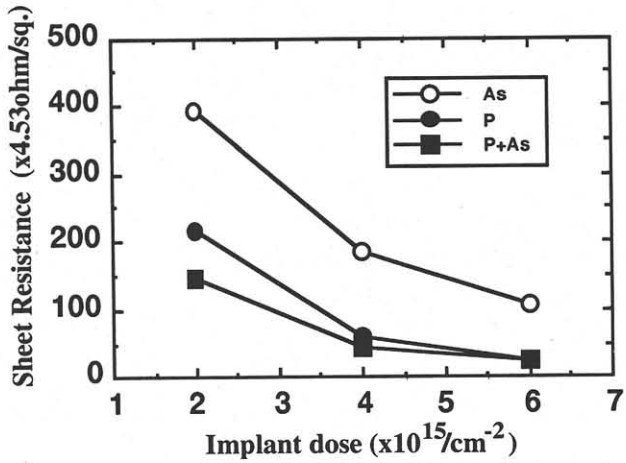

Fig.5 Sheet resistance as a function of implant dose for different implant ions.

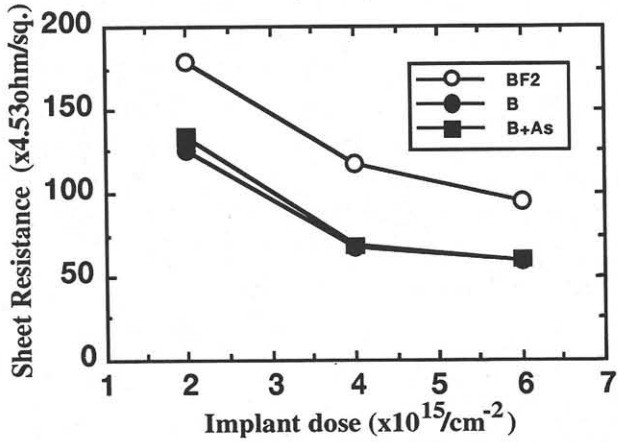

Fig.6 Sheet resistance as a function of implant dose for different implant ions.

Threshold voltage sift due to the short channel effect is shown in Fig.7 for NMOS and in Fig.8 for PMOS. The threshold voltage lowering is occurred at a effective channel length of 0.4μm for phosphorous and 0.3μm for arsenic source/drain. The threshold voltage lowering is observed at a effective channel length of 0.3μm for boron and BF_2 source/drain.

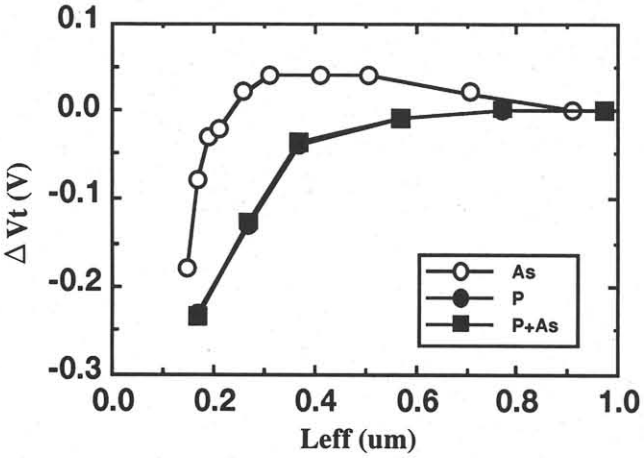

Fig.7 Threshold voltage shift due to short-channel effect.
Δ Vt=Vt(Leff)-Vt(Leff=1um) Vd=2.5(V)

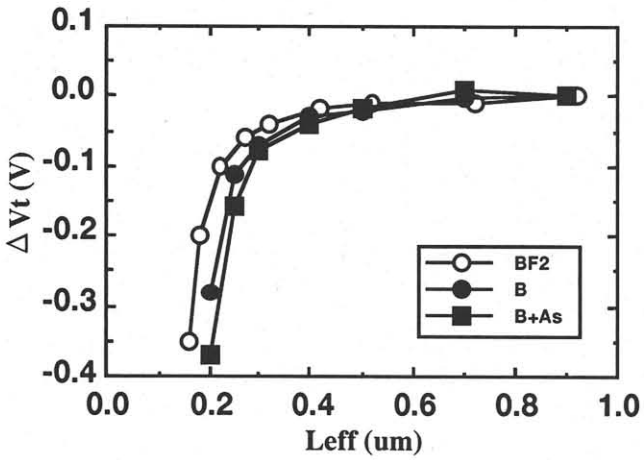

Fig.8 Threshold voltage shift due to short-channel effect.
Δ Vt=Vt(Leff)-Vt(Leff=1um) Vd=2.5(V)

The drain saturation currents for NMOS at Vd=2.5V, Vg=Vt+2.0V are shown in Fig.9. The saturation current using phosphorous ion is higher than that of arsenic ion. The drain saturation currents for PMOS at Vd=-2.5V, Vg=Vt-2.0V are shown in Fig.10. The saturation current using boron ion is higher than that of BF_2 ion. These higher current drivability for NMOS and PMOS is due to suppression of polysilicon depletion in the gate electrode formed by using phosphorous and boron ion.

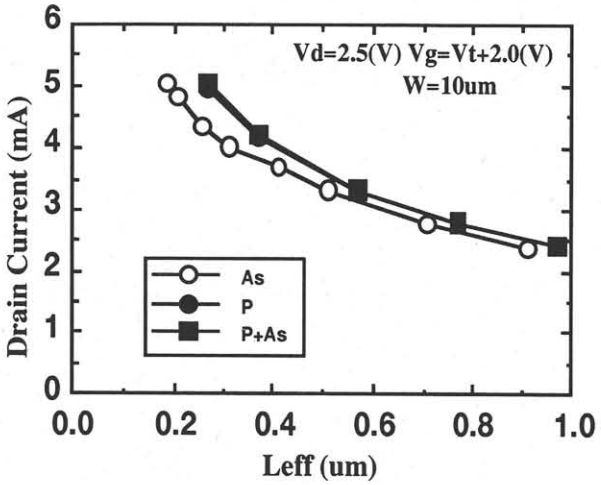

Fig.9 Drain saturation current as a function of effective channel length for different implant ions.

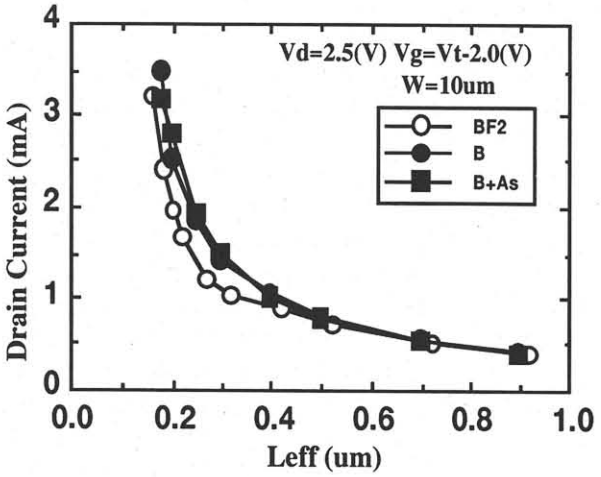

Fig.10 Drain saturation current as a function of effective channel length for different implant ions.

4. Conclusion

We have proposed a novel dual gate CMOS technology using low energy phosphorous/boron ions and arsenic pre-amorphization. This process allows a sub-quarter micron dual-gate CMOS with high current drivability, suppressing both boron penetration and polysilicon depletion effect.

Acknowledgements

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