A Concise Narrow-Channel Effect Model for Sub-Quarter-Micron SOI PMOS Devices Suitable for CAD of SOI CMOS ULSI Circuits

J. B. Kuo and K. W. Su
Rm. 338, Dept. of Electrical Eng., National Taiwan University
Roosevelt Rd. Sec. 4, Taipei, Taiwan 106-17
Fax:886-2-363-6893, Phone:886-2-363-5251x338, Email:jbkuo@cc.ee.ntu.edu.tw

Abstract
The paper reports for the first time an analytical narrow-channel effect threshold voltage model for mesa-isolated ultra-thin SOI inversion-mode and accumulation-mode PMOS devices based on a quasi-2D approach. Based on the study, contrary to inversion-mode devices, the threshold voltage of mesa-isolated ultra-thin SOI accumulation-mode PMOS devices shrinks as the channel width scales down as a result of the buried-channel effect influenced by the sidewall via the buried-oxide.

Summary
As for bulk CMOS devices [1], in sub-quarter-micron SOI CMOS devices, small-geometry effects including short-channel and narrow-channel effects [2] are important in determining their circuit performance. For ultra-thin SOI CMOS devices, mesa isolation technology offers advantages in high integration densities [3]. Sidewall-related narrow-channel effect in mesa-isolated inversion-mode ultra-thin SOI MOS devices has been reported [4].

In this paper, a concise SOI PMOS narrow-channel effect model suitable for CAD of SOI CMOS ULSI circuits is described. Fig. 1 shows the cross section of the mesa-isolated ultra-thin SOI PMOS device with the sidewall structure. Figs. 2 show the 2D electrostatic potential contours at an interval of 0.05V in the ultra-thin SOI (a) inversion-mode and (b) accumulation-mode PMOS devices as shown in Fig. 1, biased at their threshold voltages. As shown in the figures, in the inversion-mode device, the sidewall structure has a direct impact on the thin film region near the sidewall. In the accumulation-mode device, the influence of the sidewall is overwhelmed by the buried channel above the buried-oxide. Using a quasi-2D approach for both...
the inversion-mode [5] and the accumulation-mode devices and using a Gauss box approach as shown in Fig. 3 to consider the buried-channel effect for the accumulation-mode device, the narrow-channel effect threshold voltage models for the inversion-mode and the accumulation-mode devices are obtained.

Figs. 4(a)-(b) show the threshold voltage deviation vs. the channel width of the mesa-isolated ultra-thin SOI PMOS device based on the analytical model and the 2D simulation results. As seen in Figs. 4(a)-(b), the model results with $\gamma = 1$ for the inversion-mode and $l_{ox2} = 880\text{Å}$ for the accumulation-mode show a good prediction of the narrow-channel behavior for various doping densities and thicknesses of the thin-film and the buried-oxide. With a smaller channel width, the threshold voltage of the inversion-mode PMOS device becomes larger but that of the accumulation-mode one becomes smaller. As indicated in Fig. 4(a), with a thinner thin-film, the narrow-channel effect is less serious. As shown in Fig. 4(b), with a thicker buried-oxide, the narrow-channel effect is more serious for the accumulation-mode device. On the contrary, for the inversion-mode device, the narrow-channel effect is not sensitive to the thickness of the buried-oxide. The more sensitivity of the narrow-channel effect for the accumulation-mode device is due to the buried-channel structure and its influence from the buried-oxide.

Fig. 5 shows the electrostatic potential in the vertical direction in the center of the thin-film in the inversion-mode SOI PMOS device shown in Fig. 1. As shown in the figure, the model results predict well. With a thinner thin-film, the influence of the sidewall on the electrostatic potential is smaller.
Inversion Mode: \( W = 0.4 \mu m \)
\( V_G = -1.0 V \)
\( V_D = -0.1 V \)

Accumulation Mode: \( W = 0.4 \mu m \)
\( V_G = -0.35 V \)
\( V_D = -0.1 V \)

**Figure 6:** The electrostatic potential and the hole density in the vertical direction in the center of the thin-film in the ultra-thin SOI accumulation-mode PMOS device.

**Figure 7:** Subthreshold characteristics of the accumulation-mode and inversion-mode SOI PMOS devices.

Fig. 6 shows the electrostatic potential and the hole density in the vertical direction in the center of the thin-film in the ultra-thin SOI accumulation-mode PMOS device. In the accumulation-mode device, it has a buried channel above the buried-oxide. As the channel width shrinks, the buried channel moves toward the surface as influenced by the sidewall structure via the buried-oxide.

Fig. 7 shows the subthreshold characteristics of the SOI accumulation-mode and inversion-mode SOI PMOS devices as described in Fig. 1 based on 3D device simulation results. As shown in the figure, the subthreshold current of the inversion-mode device is nearly insensitive to the narrow channel effect. On the other hand, the subthreshold current of the accumulation-mode device is sensitive to the narrow channel effect. The more narrow-channel effect on the subthreshold current of the accumulation-mode device can be understood by considering the 3D hole density distribution in the devices as shown in Fig. 8. For the inversion-mode device, the subthreshold current is via the channel area near the sidewall— the subthreshold current is almost independent of the channel width. On the other hand, for the accumulation-mode device, the subthreshold current is via the buried channel in the center channel region. As a result, the width of the center channel influences the subthreshold current.

**Conclusion**

In this paper for the first time an analytical narrow-channel effect threshold voltage model for mesa-isolated ultra-thin SOI inversion-mode and accumulation-mode PMOS devices based on a quasi-2D approach has been reported. Based on the study, contrary to inversion-mode devices, the threshold voltage of mesa-isolated ultra-thin SOI accumulation-mode PMOS devices shrinks as the channel width scales down as a result of the buried-channel effect influenced by the sidewall via the buried-oxide.

**References**