Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 296-298

Effect of Nitride Sidewall Spacer on Hot Carrier Reliability Characteristics of MOSFET's

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Abstract

In this paper, we have compared the reliability characteristics of MOSFET with nitride sidewall and oxide sidewall spacer. We found the unique reliability characteristics of nitride sidewall spacer device. At the initial stage of stress, large degradation of drain current occurs for nitride sidewall device at low stress drain bias due to the enhanced trapping of nitride spacer. However, nitride sidewall devices exhibit improvement of device lifetime which was defined as a 10% degradation of drain current.

1. Introduction

For giga bit DRAM fabrication processes, Self Aligned Contact (SAC) process is necessary to improve process margin [1]. For SAC process, the difference of etch rate between oxide and nitride was used to define contact area. For this purpose, CVD Si_3N_4 layer was used as a spacer material instead of conventional CVD oxide layer. However, the extensive reliability study of deep submicron MOSFET with nitride sidewall spacer has not yet been reported. In this paper, we have compared the reliability characteristics of MOSFET with nitride sidewall and oxide sidewall spacer. We found the unique reliability characteristics of nitride sidewall spacer device. At the initial stage of stress, large degradation of drain current occurs for nitride sidewall device at low stress drain bias due to the enhanced trapping of nitride spacer.

2. Experimental Details

Conventional twin-well CMOSFETs with 8nm-thick gate oxide were fabricated on 8-inch silicon wafer. After etching various gate lengths (L_g = 0.25 - 20 μm), gate reoxidation was performed at 850°C to grow approximately 7nm-thick oxide on Si wafer. The dose and energy of As LDD ion implantation were $3x10^{13}/cm^2$, and 40keV. For sidewall spacer, 100nm-thick CVD Si_3N_4 or CVD SiO_2 were deposited respectively, and then anisotropically etched. After high dose source/drain ion implantation, heat treatment was performed at 850°C for 30min.

3. Results

It is known that high dielectric constant of nitride sidewall spacer affects channel electric field. To monitor channel electric field, impact ionization rate was measured as a function of gate bias [2]. Fig.1 shows impact ionization rate (I_{sub}/I_d) versus gate bias for 0.35μm nMOSFET with oxide and nitride sidewall spacer. Both devices exhibit almost the same impact ionization rate at the drain bias of 4.8V. This behavior can be explained by LDD structure. Because of fully overlapped LDD structure, the effect of nitride spacer on channel electric field is negligible.

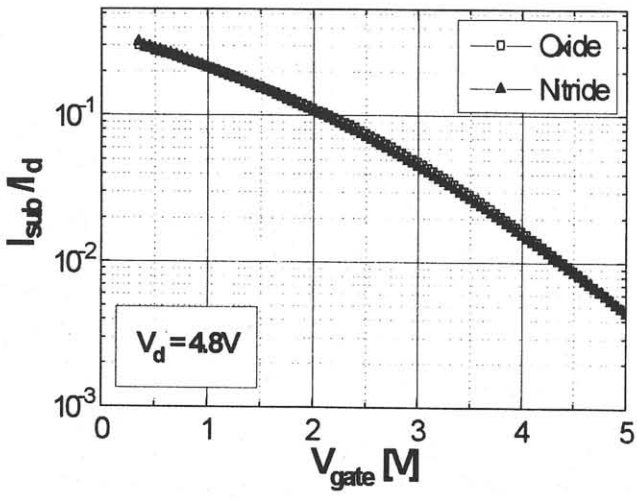

Fig.1 Impact ionization rate (I_{sub}/I_d) versus gate bias for 0.35μm nMOSFET with oxide and nitride sidewall spacer.

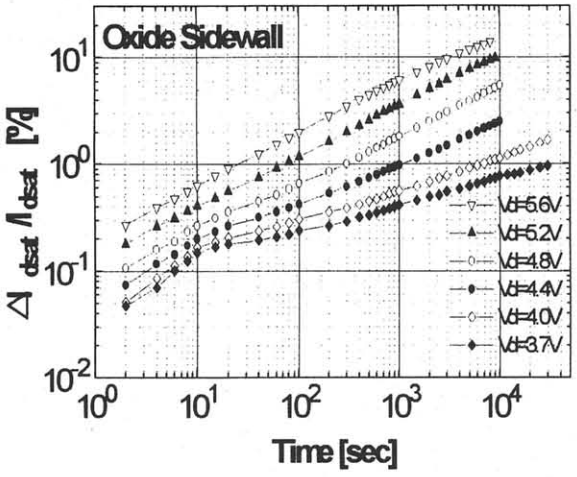

Fig. 2 The degradation of saturation drain current under various stress drain biases for oxide sidewall devices.

To compare device reliability of both devices, hot carrier stress was performed at maximum substrate current condition with various drain biases. Fig. 2 shows degradation of saturation drain current under various stress drain biases versus stress time for oxide sidewall devices. Except for the drain bias below 4V, linear correlation between $\Delta I_d/I_d$ and stress time was observed. In addition, with decreasing drain bias, significant reduction of degradation rate was observed.

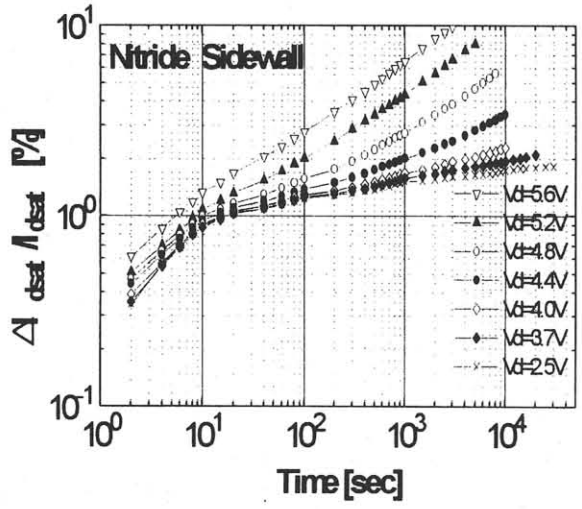

Fig. 3 The degradation of saturation drain current under various stress drain biases for nitride sidewall devices.

Fig. 3 shows degradation of saturation drain current under various stress biases for nitride sidewall devices. Compared with oxide sidewall device, the degradation behavior is drastically different for nitride sidewall device.

The degradation rates of nitride sidewall devices are significantly higher at low drain bias and initial stage of stress. With increasing stress time, the degradation rate of drain current exhibits saturation behavior.

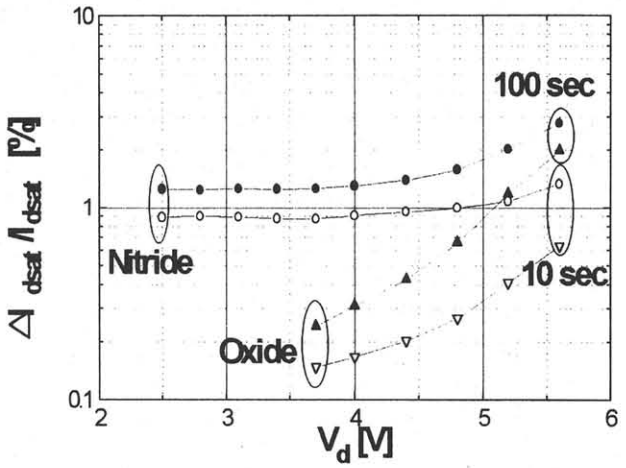

Fig. 4 The degradation of drain current after hot carrier stress for oxide and nitride sidewall spacer.

Fig. 4 shows degradation of drain current after hot carrier stress versus drain bias for oxide and nitride sidewall spacer. Significant degradation was observed after 10 sec for nitride sidewall device. In addition, the drain bias dependence of nitride sidewall devices is significantly lower than that of oxide sidewall devices. The strong drain bias dependence of oxide sidewall device is mainly due to channel electric field. With decreasing drain bias, the generation of interface state decreases significantly due to less generation of hot electron.

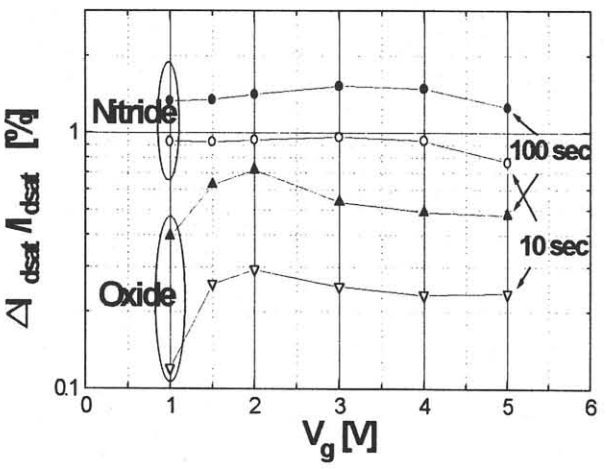

Fig. 5 The degradation of drain current versus gate bias under fixed stress time.

Fig. 5 shows drain current degradation versus gate bias under fixed stress time. For oxide sidewall device, peak degradation occurs at maximum substrate current condition. However, degradation of nitride sidewall devices versus gate bias dose not exhibit bell-shaped behavior. The weak drain and gate bias dependence of nitride sidewall device can be explained by enhanced charge trapping and low energy barrier height. It is known that the number of trap site for nitride spacer is much larger than that for oxide spacer. Since the energy barrier height of nitride sidewall spacer is relatively lower than that of oxide sidewall device, the drain and gate bias dependence of device degradation is significantly lower for nitride sidewall device. Due to charge trapping and low energy barrier height, the unique degradation behavior of nitride sidewall device can be explained.

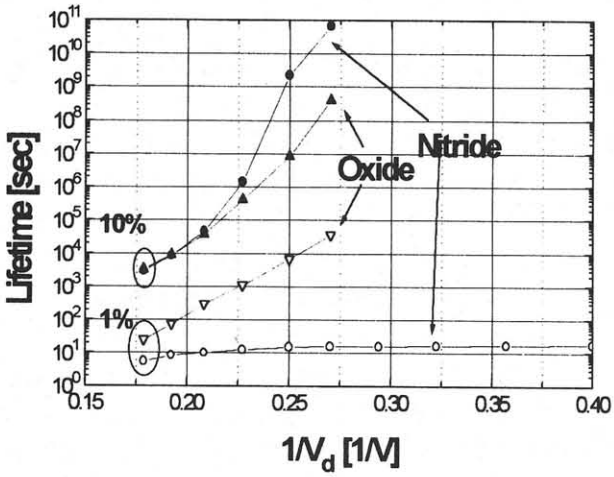

Fig. 6 The device lifetime ($\Delta I_{dsat}/I_{dsat}$ = 1% & 10%) versus drain bias for both devices.

Fig. 6 shows device lifetime ($\Delta I_{dsat}/I_{dsat}$ = 1% & 10%) versus inverse of drain bias for both devices. For 1% drain current degradation as a device lifetime criterion, significantly lower device lifetime was observed for nitride sidewall device. This can be explained by enhanced degradation of nitride sidewall device at the beginning of stress. However, nitride sidewall devices exhibit improvement of device lifetime which was defined as a 10% degradation of drain current.

4. Conclusions

In summary, we have evaluated the reliability characteristics of nitride sidewall device. We found significant initial degradation of nitride sidewall device due to charge trapping. However, the degradation rate of drain current for nitride sidewall devices exhibits saturation behavior. To obtain accurate device lifetime, it is necessary to consider the unique degradation behavior of nitride sidewall device.

Reference

1) K. P. Lee et al., IEEE IEDM Tech. Dig. (1995) 907.
2) C. Hu et al., IEEE Trans. Electron Devices, **32** (1985) 375.