Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 299-301

Sb Multiple Ion Implanted Channel for Low V_{th}, Deep Submicron SOI-pMOSFETs

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Abstract We proposed a channel doping technology for pMOSFETs in which Sb is multiply ion implanted to form a uniform doping profile after the minimum R_p of the multi-ion implantation. We derived a threshold voltage model and showed how to achieve this doping profile. This process was verified with experimental data. We fabricated SOI-pMOSFETs with the proposed channel profile and demonstrated that this device had good Vth controllability and short channel effect immunity, down to a gate length of 0.1 μm.

1. Introduction

To improve short channel immunity, scaling theory requires increasing channel doping concentration with decreasing gate length. However, a high channel doping concentration also increases the threshold voltage V_{th}. When the supply voltage is much larger than V_{th}, this increase in threshold voltage was of much concern. However, with gate lengths of 0.1 μm, the supply voltage nears 1 to 1.5 V [1], and the increase in V_{th} significantly degrades device performance.

Recently, we proposed counter doping into a uniformly and heavily doped channel, as shown in Fig.1 (a). We derived a threshold voltage model for this device and demonstrated superb short channel immunity in the L_G of less than 0.1 μm. This technology was successfully applied to nMOSFETs because we can use the counter dopant of Sb, which provides a sharp ion-implanted profile, to maintain its profile during thermal processing due to its low diffusion coefficient [2], [3].

However, the application of this technology to pMOSFETs is difficult because the candidates for counter dopant are B and In. B has high diffusion coefficient and In has a low active fraction [4].

Therefore, we proposed a channel doping profile for pMOSFETs using Sb multiple ion implantation, where the profile is uniform in the region deeper than the projected range of the ion implanted profile of lower ion implantation energy, as shown in Fig. 1 (b). This technology has the same effect on device characteristics as that of the proposed counter doping technology.

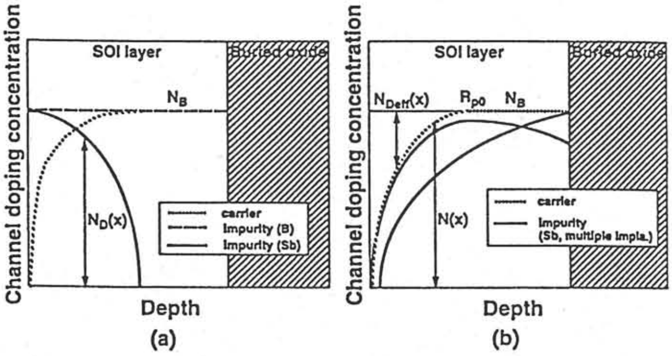

Fig. 1. (a) Counter doping profile [3]. (b) Proposed channel doping profile.

2. Threshold voltage model

We assume the channel doping profile as shown in Fig. 1 (b). The threshold voltage of counter doping into uniformly and heavily doped channel region was derived in [2], [3]. This channel profile can be also regarded as the same as a uniformly doped and ion-implanted profile obtained by different type of doping, $N_{Deff}(x)$.

We assume nMOSFET in the derivation of models for counter doping in [2] and [3], and hence we regard this device as nMOSFET and derive models for nMOSFETs. The model is easily converted for pMOSFETs by appropriately changing the sign and dopant type. The feasibility of this channel doping profile will be discussed later.

We assume a low concentration substrate, and neglect the concentration. The doping concentration in Fig. 1 (b) is expressed by

$$N=\begin{cases} N_B \exp\left[-\dfrac{(x-R_{p0})^2}{2\Delta R_p^2}\right] & (x \le R_{p0}) \\ N_B & (x \ge R_{p0}) \end{cases}.$$

The effective background doping concentration is N_B, and the subtraction of N from the effective background doping concentration is regarded as the counter doping. This effective counter doping concentration N_{Deff} is given by

$$N_{Deff}=N_B-N$$
$$=\begin{cases} N_B\left[1-\left\{-\dfrac{(x-R_{p0})^2}{2\Delta R_p^2}\right\}\right] & (x \le R_{p0}) \\ 0 & (x \ge R_{p0}) \end{cases}.$$

The effective centroid R_{peff} and effective dose Φ_{Deff} are then given by

$$R_{peff}=\frac{\int_0^\infty xN_{Deff}dx}{\int_0^\infty N_{Deff}dx}, \quad \phi_{eff}=\int_0^\infty N_{Deff}dx .$$

The threshold voltage V_{th} is given by

$$V_{th}=V_{FB}+2\phi_F+\frac{Q_{B0}}{C_{ox}}\left[\sqrt{1+\frac{2R_{peff}}{W_0}\left(\frac{Q_{Deff}}{Q_{B0}}\right)}-\frac{Q_{Deff}}{Q_{B0}}\right],$$

where V_{BF} is the flat band voltage, C_{ox} is the gate capacitance per gate area, and ϕ_F is given by

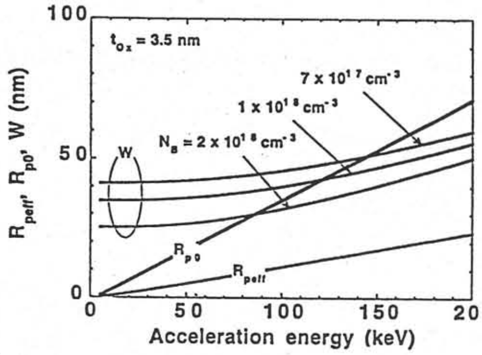

Fig. 2. Dependence of R_{peff}, R_{po}, and W on accelerat energy .

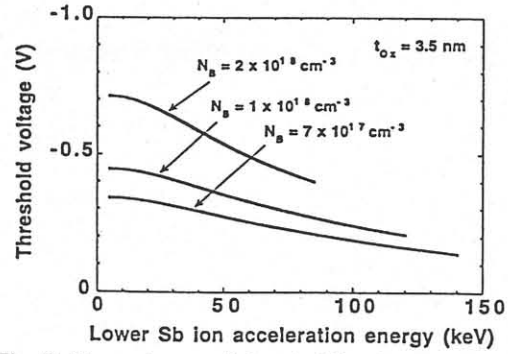

Fig. 3. Dependence of threshold voltage on acceleration energy with various background doping concentrations of N_B.

$$\phi_F=\frac{k_BT}{q}\ln\left(\frac{N_B}{n_i}\right) .$$

W_0 is the depletion width with the uniform profile channel given by

$$W_0=\sqrt{\frac{2\varepsilon_{Si}(2\phi_F)}{qN_B}} .$$

Q_{B0} and Q_{Deff} are given by

$$Q_{B0}=qW_0N_B$$

$$Q_{Deff}=q\Phi_{Deff} .$$

The depletion width W of this doping profile is given by

$$W=W_0\sqrt{1+\frac{2R_{peff}}{W_0}\left(\frac{Q_{Deff}}{Q_{B0}}\right)} .$$

Fig. 2 shows the relationship between the depletion width W and R_{p0}, R_{peff}. The theory is valid when $W > R_{p0}$. As N_B increases, the available minimum acceleration energy is small.

Fig. 3 shows the dependence of V_{th} on the acceleration energy. When we use the threshold voltage of 0.3 V, the maximum N_B is between 1 x10^{18} and 2x 10^{18} cm^{-3}.

3. Condition of Sb multiple ion implantation

Multiple ion implantation is sufficient to achieve the proposed profile when we use an SOI substrate of 100 nm which is the typical thickness for partially depleted devices.

To obtain fundamental data for determining the conditions necessary to obtain a desired V_{th}, we evaluated Sb ion-implanted profiles with an energy range of between 20 and 340 keV. Some of the profiles are shown in Fig. 4. The profile is asymmetrical and, therefore, we extracted parameters of a jointed half Gaussian distribution [5]. The parameters for the jointed half Gaussian distribution is extracted as follows. First, R_{pm} is evaluated at the point of maximum doping concentration, then the standard deviations ΔR_{pf} ($x<R_{p0}$), ΔR_{pb} ($x<R_{p0}$) are evaluated.

Fig. 5 shows the extracted parameters; each parameters closely fits the a linear function of acceleration energy E. Fig. 4 compares the analytical and experimental data, and it shows good match.

4. SOI-pMOSFET fabrication and characteristics

To verify our threshold voltage model, we fabricated the pMOSFET using EB lithography.

Sb was ion-implanted into 100 nm thick SOI with the conditions given in the Table I. After 3.5-nm-thick gate oxidation, the conventional pMOS process with a p^+ polysilicon gate was followed.

Fig. 6 shows the SIMS Sb profiles after final thermal processing. The profile is uniform after R_{p0} as was expected, and agrees well with the theoretical data in which the parameters representing ion implantation are used.

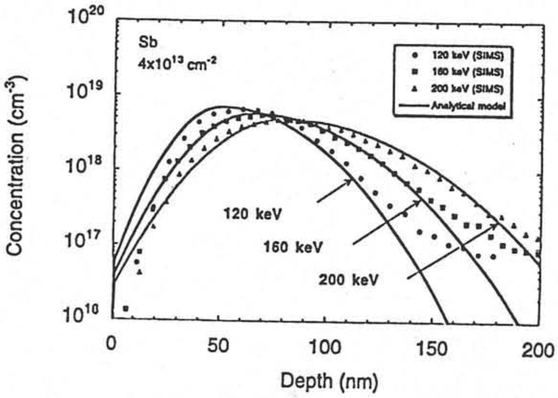

Fig. 4. SIMS Sb concentration profiles with various acceleration energies. The analytical data with jointed-half Gaussian distribution profiles is also shown.

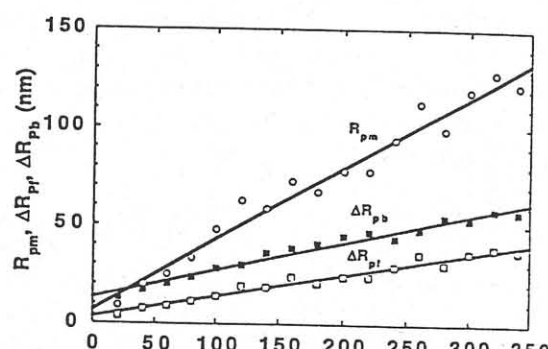

Fig. 5. Extracted parameters for Sb ion implanted profiles.

Table I. Multiple ion implantation conditions and associated threshold voltage.

Device number	Sb II-1	Sb II-2	N_B	V_{th} (Theory)	V_{th} (Experiment)
1	120 keV, 4.9 x 10^{12} cm^{-2}	347 keV, 1.4 x 10^{13} cm^{-2}	1 x 10^{18} cm^{-3}	- 0.20 V	- 0.25 V
2	70 keV, 3.7 x 10^{12} cm^{-2}	236 keV, 1.2 x 10^{13} cm^{-2}	1 x 10^{18} cm^{-3}	- 0.30 V	- 0.37 V
3	85 keV, 8.1 x 10^{12} cm^{-2}	269 keV, 1.1 x 10^{13} cm^{-2}	2 x 10^{18} cm^{-3}	- 0.40 V	- 0.50 V
4	120 keV, 9.9 x 10^{12} cm^{-2}	346 keV, 8.3 x 10^{12} cm^{-2}	2 x 10^{18} cm^{-3}	- 0.30 V	- 0.38 V

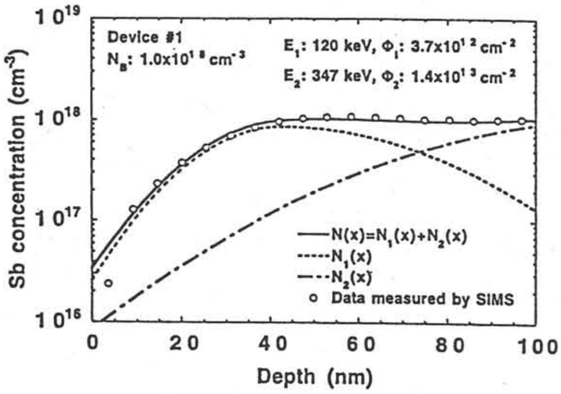

Fig. 6. Comparison of the experimental and analytical channel doping concentration profiles.

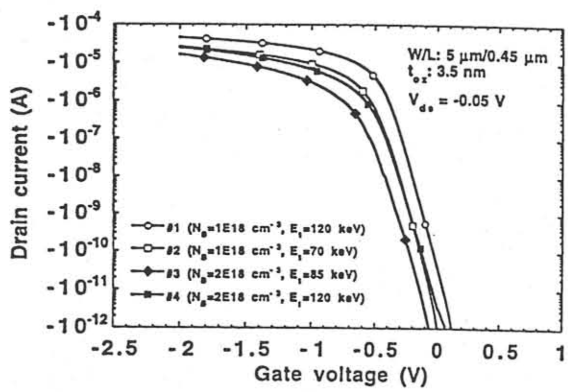

Fig. 7. Subthreshold characteristics.

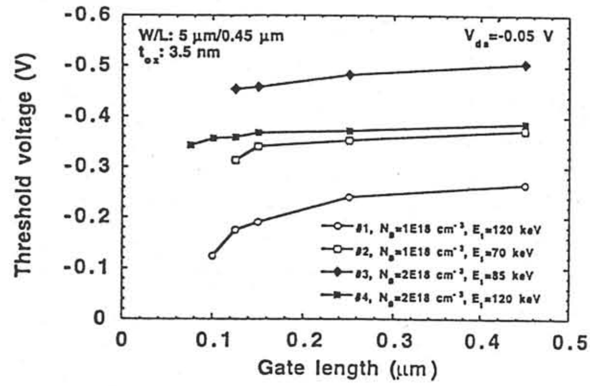

Fig. 8. Dependence of threshold voltage on gate length.

Fig. 7 shows the subthreshold characteristics of the device. V_{th} was evaluated by linear extrapolation from the bias points at the maximum transconductance. As shown in Table I, the experimental V_{th} closely agrees with the analytically obtained values, proving the validify of our V_{th} model.

Figure 8 shows V_{th} as a function of gate length for different channel profiles. With a gate oxide thickness of 3.5 nm, the SCEs are adequately suppressed with a gate length of down to 0.1 μm, while maintaining a low V_{th} for the proposed channel profiles. The characteristics are the same as those of counter-doped nMOSFETs previously reported [9],[10]. From the above results, deep submicron, low V_{th} SOI-CMOS without SCEs can be fabricated for high-speed operation at a low supply voltage.

5. Conclusion

We proposed multiple Sb ion implantation for the pMOS channel, in which the profile is uniformly deeper than the projected range of the lower acceleration energy. We also derived the threshold voltage model and extracted parameters of implanted profiles.

We demonstrated the feasibility of the proposed channel profile experimentally, by fabricating deep sub-micron SOI-pMOSFETs. We verified the validity of the threshold voltage model and that the SCEs are adequately suppressed with gate lengths of down to 0.1 μm, while maintaining a low V_{th} for the proposed channel profiles.

Acknowledgments

We gratefully thank to Mr. Fukano and members of the device fabrication group for fabrication of the SOI-pMOSFETs.

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