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Reduction of Charge Build-up during Reactive Ion Etching by Using SOI Structures

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The charge build-up of SOI structures during reactive ion etching has been investigated. The charge build-up was evaluated by using MNOS capacitors fabricated on SOI. It has been found that the charge build-up can be drastically reduced by using SOI, while the etching rate is almost similar to the use of bulk Si wafers. Dependence of the charge build-up on buried SiO_2 thickness has been investigated. A model to explain these phenomena is discussed.

1. INTRODUCTION

One of the critical issues in further shrinkage of device dimension and further integration of devices is the charge build-up during reactive ion etching (RIE) which causes the gate breakdown of MOS devices and etching profile distortion. [1,2] There are two main approaches to minimize the charge build-up. One is the optimization of plasma parameters for reducing the charge build-up. From this point of view, we have found that the use of electronegative gases such as CF_4 and O_2 results in pronounced charge build-up, and that the addition of H_2 gas to these electronegative gases results in remarkable reduction of the charge build-up.[3] The other approach is the design of device structures to reduce the charge build-up.[4] In this paper we report that the use of silicon-on-insulator (SOI) structures is very effective in reducing the charge build-up during RIE without reducing the etching rate. The results to be presented includes the required thickness of the buried insulator and a model to explain the reduction in charge build-up by the use of SOI.

2. EXPERIMENTAL

Metal/ nitride/ oxide/ silicon (MNOS) capacitors were used to evaluate charge build-up. The structure of this test device is shown in Fig. 1. SOI wafers were prepared by direct bonding of bare and oxidized wafers.

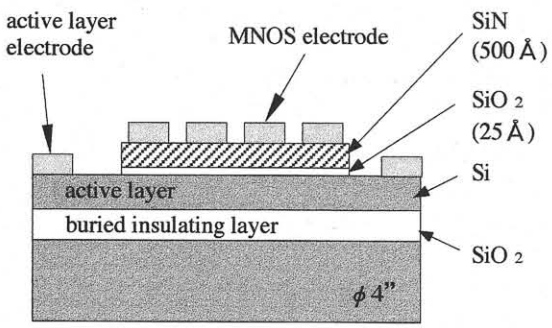

Fig. 1: Schematic cross section of MNOS capacitors on SOI.

In order to investigate dependence of charge build-up on buried insulator thickness, SOI wafers having buried SiO_2 ranged from 0.3 μm~2.9 μm in thickness were prepared. Detail of wafer bonding condition is listed in Table 1. A parallel plate type reactive ion etching (RIE) system was used. Plasma was generated by applying radio frequency (13.56MHz) power. Gas used was O_2. Detail of plasma treatment condition is listed in Table 2.

The flat-band voltage shift (ΔVfb) of the MNOS capacitors was measured by the capacitance-voltage (C-V) measurement. The ΔVfb of an MNOS capacitor as a function of applied dc

Wafer size	ϕ 4 inch
Thickness of oxide	0.31, 0.45, 1.9, 2.9 μm
Anneal temperature	1050℃
Anneal time	2 hours
Etching condition	HF:HNO_3:CH_3COOH =175: 350: 175ml

Table 1: Wafer bonding condition.

Gas	O_2
Rate of gas	50 sccm
RF power	50 W (80mW/cm)^2
RF frequency	13.56 MHz
Time	60 sec
Pressure	7 Pa

Table 2: Plasma treatment condition.

gate voltage is shown in Fig. 2. MNOS capacitors were repeatedly used by applying a delete voltage (Vdelete) of -30V to each MNOS capacitors prior to exposure to plasma. Fig. 3 shows ΔVfb of an MNOS capacitor observed by repeatedly applying Vwrite=+10V and Vdelete=-30V to the gate electrode for thirty times. We can see that ΔVfb almost stays at a constant value for the period. This demonstrates that the repeated use of MNOS capacitors is very effective to improve the accuracy and the reproducibility of the evaluation of the charge build-up at various conditions.

In order to evaluate the effectiveness of the use of SOI, Δ Vfb of the two wafer setups were compared (Fig. 4): One is the ΔVfb obtained from SOI (ΔVfbSOI). The other is the ΔVfb obtained by electrically connecting the active layer of SOI to the cathode of RIE system. This wafer set up is electrically equivalent to the situation in which a conventional bulk Si wafer is employed. In fact ΔVfb values obtained from this wafer setup were similar to these obtained by using bulk Si wafer. Thus we designate ΔVfb values obtained from the later wafer setup as ΔVfbBULK.

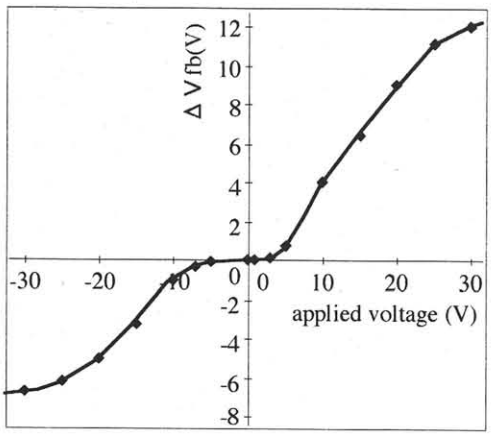

Fig. 2: The Δ Vfb of MNOS capacitors as a function of applied gate voltage.

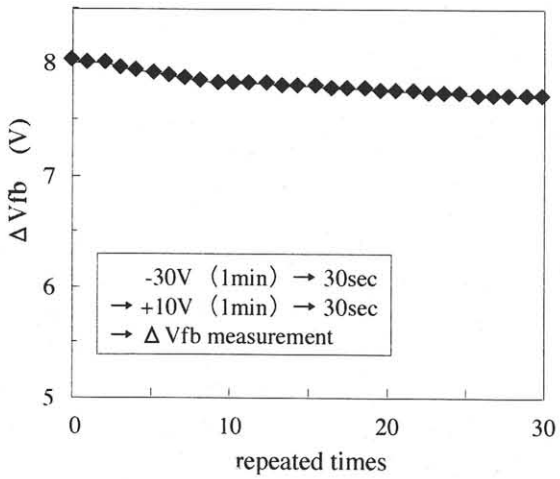

Fig. 3: Δ Vfb values measured by repeatedly applying Vwrite= +10V and Vdelete =-30V.

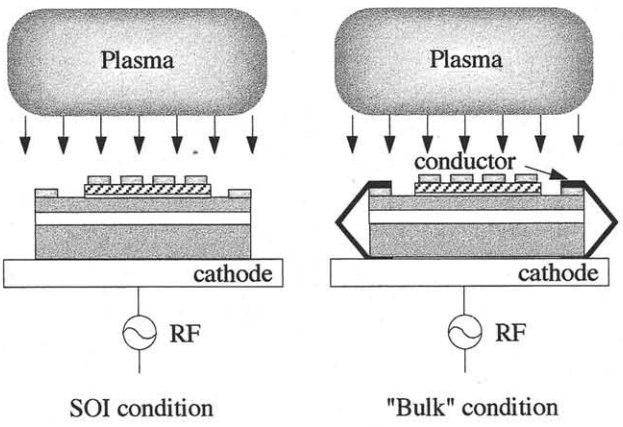

Fig. 4: Two experimental setups used for evaluation of SOI and "bulk" condition .

3. RESULTS AND DISCUSSION

Fig. 5 shows comparison between Δ VfbSOI and Δ VfbBULK for the case that the buried SiO2 is 1.9 μm in thickness. It is clear that ΔVfb can be drastically reduced by using SOI structure. Fig. 6 shows dependence of ratio Δ VfbSOI/ ΔVfbBULK on buried SiO_2 thickness. We can see from this figure that the ratio decreases with the increase of buried SiO_2 thickness. The results suggest that, by increasing the buried SiO_2 thickness to about 3 μm, the equivalent gate voltage applied to the gate during the plasma treatment can be reduced from about 25V of bulk Si wafer to only a few volt.

The reduction of charge build-up by the use of SOI can be explained by the model shown in Fig. 7. That is, SOI provides a capacitor in addition to the device (MNOS) capacitor. These capacitors are connected in series between the plasma and the cathode. Thus the effective voltage applied to the device capacitor is reduced.

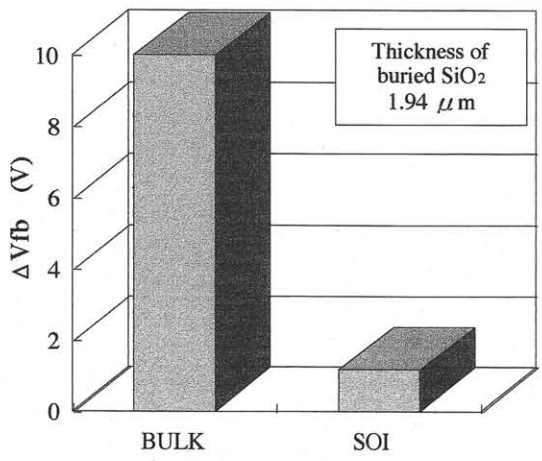

Fig. 5: Δ VfbSOI and Δ VfbBULK obtained after oxygen plasma treatment by using the RIE system.

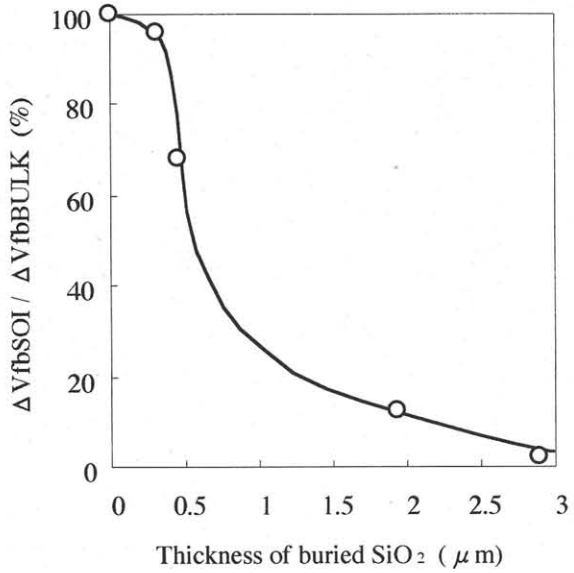

Fig. 6: ΔVfb change with thickness of buried SiO_2.

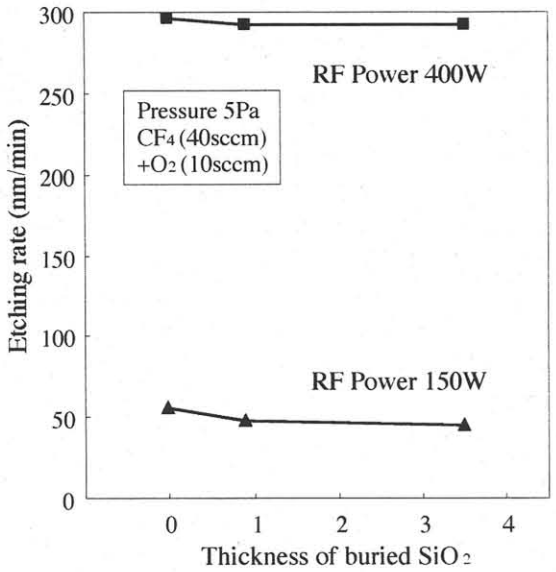

Fig. 8: Si etching rate at RF power 150W and 400W change with thickness of buried SiO_2.

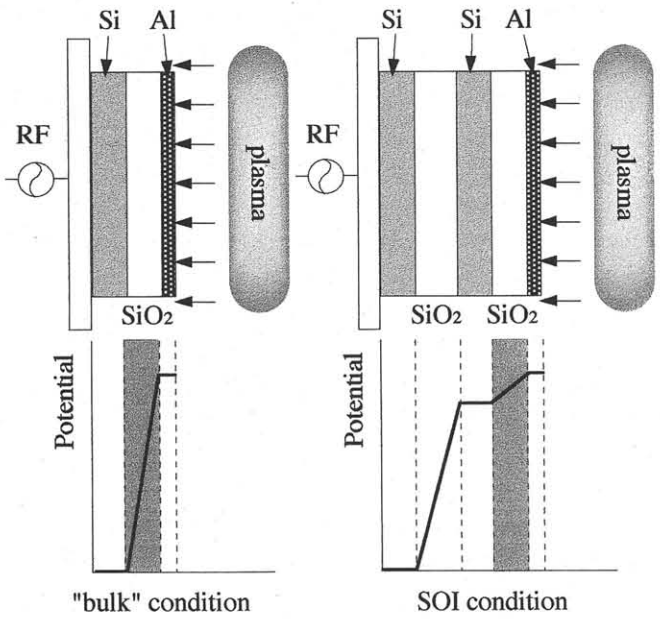

Fig. 7: Model to explain the charge build-up reduction by the use of SOI.

Next the relationship between thickness of buried SiO_2 and etching rate have been investigated. Fig. 8 shows change in Si etching rate with thickness of buried SiO_2 thickness. Gas used was CF_4(40sccm)+O_2(10sccm). The tests were carried out for RF powers 150W and 400W. We can see from this figure that etching rate at 400W is almost independent of the thickness of buried SiO_2, while ΔVfb can be drastically reduced by using SOI structure. The etching rate at 150W shows a little dependence on the thickness of buried SiO_2. This result suggests that, at low RF power, SOI slightly affect the self bias voltage Vdc since the Vdc itself is small. However, the change in etching rate with the use of SOI is very small compared with the drastical decrease of ΔVfb.

5. CONCLUSION

We conclude that the use of SOI structures is very effective in reducing the charge build-up during RIE without reducing the etching rate. The reduction of charge build-up by the use of SOI can be explained by the model that SOI provides a capacitor in addition to the device capacitor. These capacitors are connected in series between the plasma and the cathode. Thus the effective voltage applied to the device capacitor is reduced. Concerning the etching rate, it has been confirmed that the etching rate is not affected by the insulation of the active layer. The plasma condition used in this work has been found to induce a significant amount of charge build-up.[3] This work suggests that buried SiO_2 layers as thick as about 3 μm is required to reduce the equivalent gate voltage to a few volt when such severe plasma condition is encountered in the process.

References

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