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Thinning of SOI Bonded Wafers by Applying Voltage during KOH Etching

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A thinning technique for controlling thickness variation in Si-on-insulator (SOI) bonded wafers is presented. During KOH etching, voltage is applied between the supporting substrate and the etchant. The SOI thickness variation after the etch stop depends on the leakage current during etching. Reducing the current to the order of nanoamperes results in a thickness range of 50 nm. The average thickness of the superficial Si ranging from 0.3 to 2 μm was obtained by etching 3 ± 0.5-μm-thick SOI bonded wafers, and depended on the applied voltage. AFM observation reveals the surface roughness of 1.4 nm (RMS).

1. INTRODUCTION

Si-on-insulator (SOI) wafers fabricated by wafer bonding are recognized as one of the most reliable substrates for device fabrication, due to their good crystal qualities and interface characteristics[1)-3)]. With wafer bonding, however, it is difficult to produce a uniformly thin SOI active layer. Many techniques has been proposed for thinning SOI bonded wafers, such as using single and double etch stops at the epitaxial[4)], doped[5)], or porous layer[6)]; etching by plasma beam scanning[7)]; and mechanical cutting at the H^+ implanted region[8)]. However, most of the techniques include relatively high-cost processes such as epitaxy, ion implantation, dopant diffusion, and plasma etching. Moreover, these techniques occasionally introduce defects in the Si active layer or use a poor bonded interface as the active Si/buried oxide interface.

In this paper, the author presents a thinning technique involving KOH wet etching while applying voltage between the supporting substrate of the SOI bonded wafers and the etchant[9),10)]. This technique retains the advantages of wafer bonding such as the high quality active layer and buried interface. The depletion layer produced at the buried interface is expected to be an etch stop layer. After the etch stop, it is anticipated that both the SOI active layer thickness and its variation will be reduced simultaneously.

2. EXPERIMENTS

The starting material for the experiment includes commercially available 125 mmϕ SOI bonded wafers having a p^--active layer with thickness of 3 ± 0.5 μm, a 0.5-μm-thick buried oxide, and a p^--supporting substrate. Figure 1 shows the etching equipment. SOI wafers were set in a holder with two O-rings that exposed only the surface of the SOI active layer to the etchant. Voltage was applied between the back electrode which was pressed against the supporting substrate and the Pt electrode in the KOH solution.

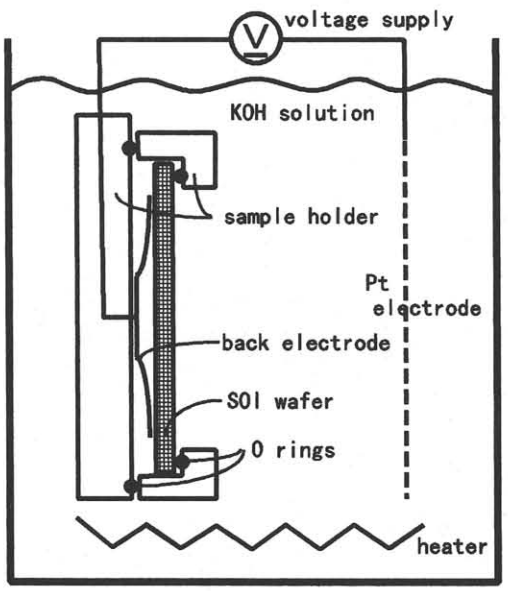

Fig. 1 Etching equipment.

Some wafers were oxidized to passivate their edges prior to etching. The samples were etched in a 20% (wt.) KOH solution at 50 to 70℃ while applying 20 to 120 V for 3 to 5 min. The leakage current during etching was measured. The SOI thicknesses and their variations were measured by optical interferometry before and after etching. For further thinning, sacrificial oxidation, which consists of thermal oxidation and subsequent HF etching of SiO_2, was carried out after the etch stop. The etched surface was also observed by AFM to evaluate the surface roughness after the etch stop.

3. RESULTS AND DISCUSSION

The average thickness obtained of the superficial Si ranging from 0.3 to 2 μm after the etch stop depended on the applied voltage.

Figure 2 shows the relationship between the current measured at the voltage supply during etching and the thickness ranges after the etch stop. Thickness range is the difference between the maximum and minimum thicknesses. In Fig. 2, clearly the SOI thickness uniformities after the etch stop improved by reducing the current during etching. Reducing the current to the order of nanoamperes resulted in a thickness range of 50 nm.

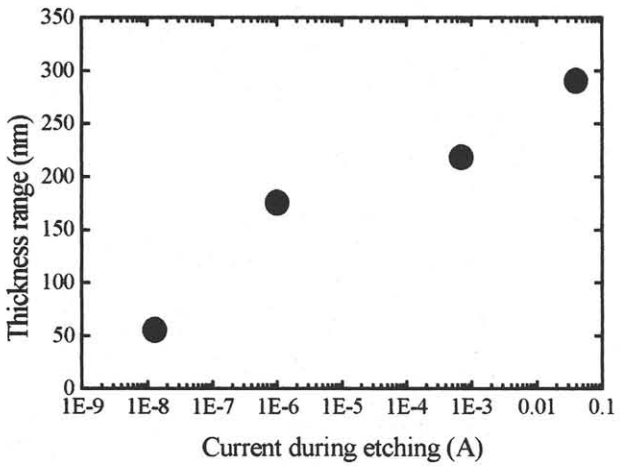

Fig. 2 Thickness ranges after etch stop versus etching current measured at voltage supply. Thickness range is defined as the difference between the maximum and minimum thicknesses.

Improving the ability of sealing the supporting substrate and the wafer edge from the etchant by carefully adjusting the height of O-rings effectively reduces the etching current. In addition, the wafer edge can be passivated by thermal oxidation to reduce the leakage current to the order of nanoamperes.

Large leakage current, especially at the wafer edge, may produce a large variation in depletion layer thickness. It is reasonable to conclude that the thickness variation after the etch stop can be improved by reducing the leakage current. To further improve SOI thickness uniformity, therefore, reducing the leakage current down to the order of picoamperes should be effective. It may also be possible to improve uniformity by refining the etching conditions, such as etching temperature and distance between the Pt electrode and the sample, for the same leakage current level.

Typical thickness variation across the 125 mmϕ wafer, measured by optical interferometry, is shown in Fig. 3. The thickness of the active Si layer is controlled within ±5% for the mean value of ~0.5 μm, with the exception of the O-ring edges where the etchant might not be sufficiently supplied. Further thinning can be achieved by combining the present etch stop and additional sacrificial oxidation. A 0.1-μm-thick SOI, fabricated by the technique described above, retained a thickness range of 50 nm (±25 nm) after sacrificial oxidation.

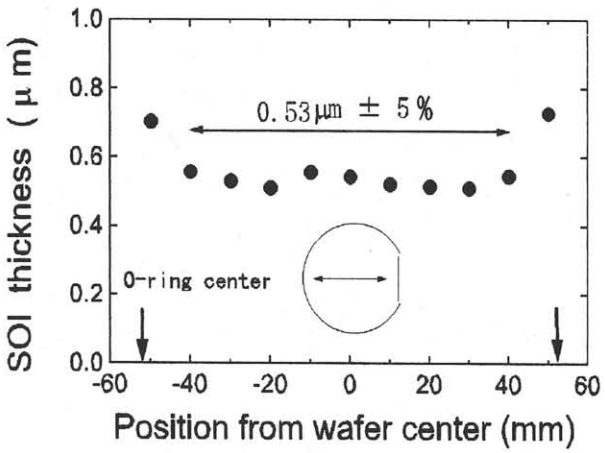

Fig. 3 SOI active layer thicknesses across 125 mmϕ bonded wafer after etch stop.

The surface roughness degraded slightly after the etch stop. Figure 4 shows the AFM image taken over a 2 μm x 2 μm area. The RMS value calculated from the AFM measurement was 1.4 nm, which is equal to or slightly

better than other thinning techniques. Therefore, the author believes that this roughness can be reduced in conjunction with techniques used in other methods, such as "touch polishing" or high-temperature annealing, to obtain the same surface smoothness as that of the state of the art bulk substrate.

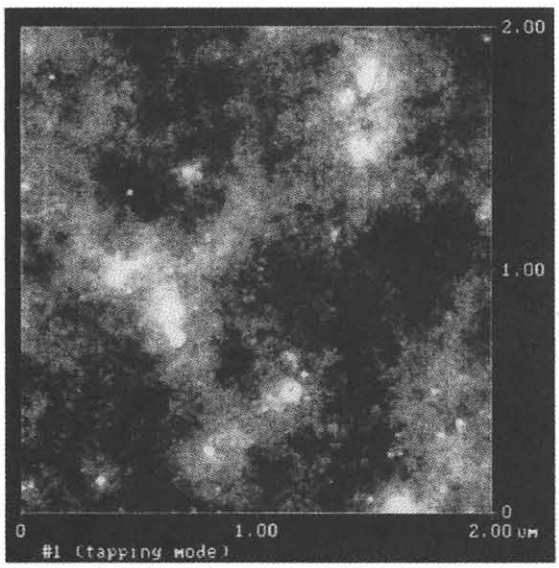

Fig. 4 AFM image of etched surface taken over a 2 µm x 2 µm area.

4. SUMMARY

In summary, a thinning technique in which voltage is applied between the supporting substrate and the etchant during KOH etching of SOI bonded wafers was presented. The SOI thickness variation after the etch stop depended on the level of leakage current during etching. Reducing the current to the order of nanoamperes, can give a thickness range of 50 nm (±25 nm). With this technique, the average thicknesses of the superficial Si ranging from 0.3 to 2 µm was obtained by etching 3± 0.5-µm-thick SOI bonded wafers, and depended on the applied voltages. Further thinning down to 0.1 µm can be achieved by combining the etch stop and additional sacrificial oxidation, with retaining thickness uniformity. AFM observation revealed that the surface roughness was 1.4 nm (RMS).

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