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A 100±15nm Thick 8-inch Bonded SOI Fabricated with a Selective Polishing Method

M. Hashimoto, Y.Ohkubo, M. Shimanoe, M. Nakamura, H.Sato, H.Komatsu and Y.Miyazawa

ULSI R&D Laboratories, Semiconductor Company, Sony Corporation
4-14-1 Asahi-cho, Atsugi-shi, Kanagawa, 243 Japan
Telephone 0462-30-5808, Fax 0462-30-5730

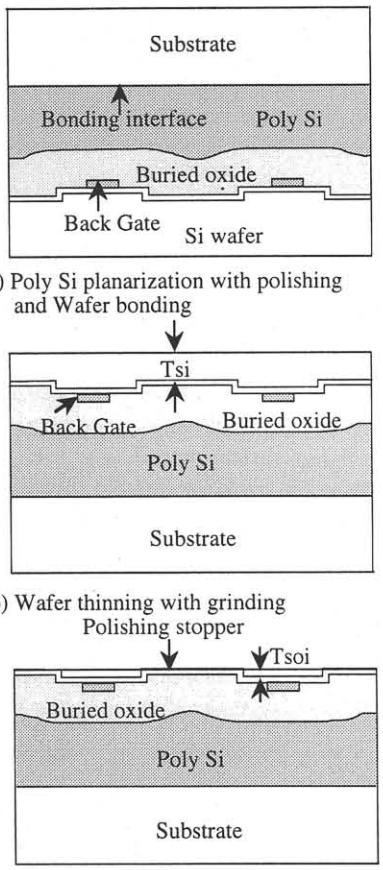
A 100±15nm thick 8-inch bonded SOI is fabricated with a selective polishing method. The process fluctuations disturbing the SOI thickness uniformity are reduced for both grinding and polishing. The polishing selectivity (rate ratio of Si on the oxide stopper to SOI) increases to 37 by optimizing polishing pressure and rotation speed conditions. The SOI thickness in a pattern less than 200 μm □, decreases due to not dishing but etching by ethylenediamine solution for the selective polishing.

1. Introduction

Thin film SOIMOS LSIs are attractive for low power and/or high speed applications. Therefore various methods to fabricate thin film SOI wafers have been proposed[1-3]. A wafer bonding and selective polishing (chemical polishing with ethylenediamine) method shown in Fig.1, is one of hopeful candidates to realize an uniform and thin SOI wafer[4-5]. An SOI fabricated with this method has high crystalline quality, and moreover the elements such as capacitors for DRAM can be buried below the SOI layer[6-7].

In a selective polishing, the oxide stopper surrounding the SOI islands, protects SOI layers from being polished. However the fluctuations of the Si thickness on the stopper before the polishing (Tsi) and the polishing rate (Rsi), still affect the SOI thickness uniformity. Increasing wafer size from 5 to 8 inches results in bigger fluctuations and worse uniformity in the SOI thickness.

In this work, it will be presented how to reduce the above fluctuations. Then the selectivities at various polishing conditions will be shown, and the selective polishing mechanizm will be discussed. A successful fabrication of a 100 ± 15nm thick 8-inch bonded SOI will be reported finally.



(a) Poly Si planarization with polishing and Wafer bonding

(b) Wafer thinning with grinding

(c) Selective polishing

Fig.1. Wafer bonding and selective polishing method

2. Basic Concept

The SOI thickness fluctuation (ΔTsoi) is expressed as

$$\Delta Tsoi \approx \frac{Rsoi}{Rsi.a}\sqrt{(\Delta Tsi)^2+(Tsi.a)^2\left(\frac{\Delta Rsi}{Rsi.a}\right)^2}$$

where Tsi : Si thickness on the stopper
Rsi : polishing rate of Si on the stopper
Rsoi : thickness decreasing rate in an SOI

and "Δ", ".a" means "fluctuation", "average" respectively. Δ Tsoi is inversely proportional to the polishing selectivity, which is defined as (Rsi.a/Rsoi). To improve Tsoi uniformity, we have to decrease Δ Tsi, Tsi.a, Δ Rsi and increase the selectivity.

Rsoi depends on the SOI pattern size in general. Therefore the SOI thickness must be always measured at same size pattern. A 30μm square pattern is used through this work.

3. Decreasing Tsi.a, Δ Tsi

As shown in Fig.1, bonded wafers are thinned with the grinding. As Tsi.a becomes thinner, the defects in the SOI layers caused by the grinding increase. Therefore, to determine the thinning limit of Tsi.a, the relation between defect density (N) and depth from the surface (s) must be known. This relations were investigated for three grinding rates (v) as follows. Si wafers were ground with SVG-202MK2 Grinding Machine. After the polishing, the wafers were oxidized for 16 hours at 1000 ℃ Then they were chemically etched with Wright Etch Solution, and the OSF defect density was measured for each wafer. The defect density (N) at the desired depth (s) can be achieved by adjusting the removed Si thickness in the polishing.

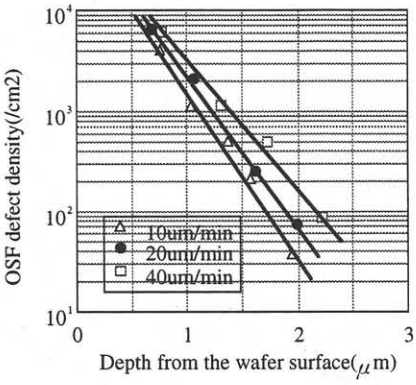


Fig.2. Defect density in the wafer after grinding (dependence on the depth)

Figure 2 shows the relations for three grinding rates (v). The relation can be expressed as follows.

$$N = No(v)\ \exp(-k(v)s)$$

No(v) means defect density at the surface. As the grinding rate decreases, k(v) in the above equation increases, but grindstones must be dressed more frequently. Considering operational efficiency and defect density, the grinding rate was fixed at 20 μm/min. The thinning limit of Tsi.a was 3μm from Fig.2, where the defect density was 1 ~2/cm2.

The thickness distribution of the ground wafer was controlled to minimize ΔTsi. The thickness distributions of the poly Si, the buried oxide and the substrate wafer (see Fig.1) were measured at 9 points before the wafer bonding. With these data, the ideal wafer thickness distribution was obtained for each wafer. The thickness distribution of the ground wafer was fitted as closely to the ideal as possible, by adjusting the grinding spindle angle. Consequently Δ Tsi could be decreased to about ± 0.6μ m in an 8-inch wafer as shown in Fig.3.

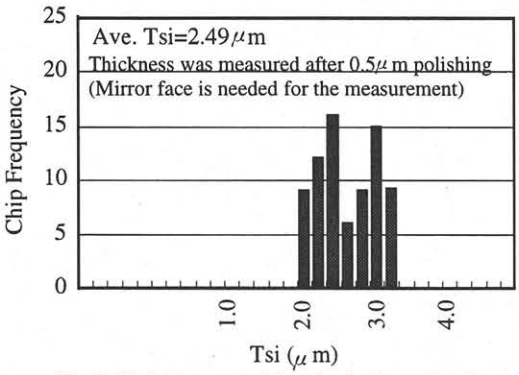
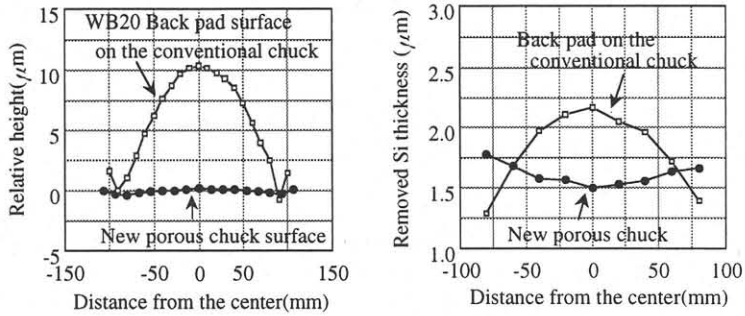


Fig.3. Si thickness uniformity before selective polishing

4. Decreasing Δ Rsi/Rsi.a

The polishing rate distribution depends heavily on either the backing pad or the chuck flatness . To decrease ΔRsi/Rsi.a, an ultra flat porous chuck was adopted, and a wafer was directly adhered to it with vacuum. Figure 4 shows the surface flatness and the polishing rate distribution along the wafer diameter for the back pad on the conventional chuck and the new porous chuck. Here SH-24-S polishing machine and SUBA800 polishing pad were used. ΔRsi/Rsi.a in an 8-inch wafer decreased to about 1/3 at the same polishing conditions.



(a) Surface flatness (b) Polishing rate distribution

Fig.4. Comparison between a back pad on the conventinal chuck and a new porous chuck

5. Increasing the selectivity

The selectivity in various polishing conditions was investigated with the same machine and pad used in the experiments at previous Section. The wafers having Tsi.a = 3 ~4 μm and ΔTsi ~ ±0.6 μm were prepared, then Rsi.a , Rsoi were measured at various pressure to the wafer (W) and polishing plate rotation speed (Rot) conditions. The concentration of ethylenediamine solution used in the polishing was fixed at 0.0005vol% and its flow rate was 60cc/min. The dependencies of both Rsi.a and Rsoi on W at a rotation speed of 30rpm, are shown in Fig.5. As W increases, Rsi.a increases linearly, while the change of Rsoi is small. The dependencies of both Rsi.a and Rsoi on Rot at a pressure of 300g/cm2, are shown in Fig.6 (the wafer holding plate had the same rotation speed as the polishing plate). Rsi.a saturates when Rot exceeds 50rpm, while Rsoi is still increasing. In these experiments, the temperature of the polishing pad surface (T) was measured with an infrared radiation thermometer. Rsoi as a fuction of T is shown in Fig.7.

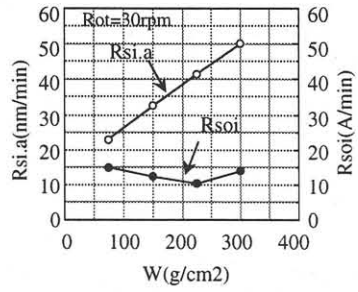


Fig.5. Rsi.a & Rsoi dependence on W

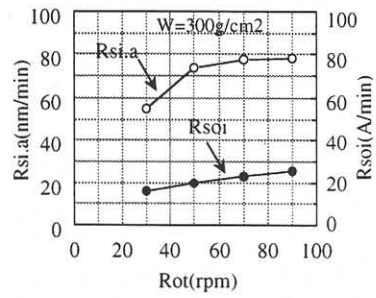


Fig.6. Rsi.a & Rsoi dependence on Rot

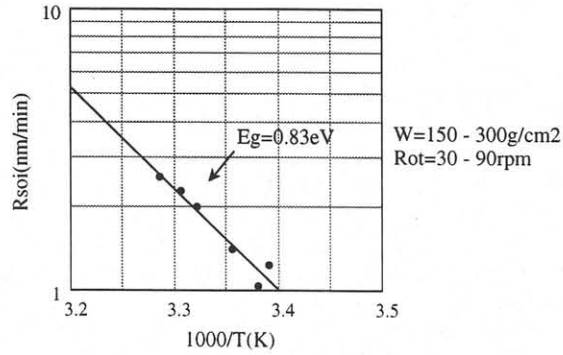


Fig.7. SOI thickness decreasing rate dependence on the pad surface temperature in the selective polishing
T=Polishing pad surface temperature

From Fig.5 and Fig.6, the polishing selectivity can be easily obtained. The optimum polishing condition, where the selectivity takes the maximum value of 37, exists at about W=300g/cm2 and Rot=50rpm. In Fig.7, Rsoi looks to be satisfying the Arrhenius equation in spite of the polishing condition difference. This result shows that the thickness decrease in an SOI is caused by a single chemical reaction. The activation energy of the reaction evaluated from Fig.7 is 0.83eV.

6. Discussion on the selective polishing

The decrease of the SOI thickness in the selective polishing has been explained with dishing effect until now. According to this idea Rsoi must increase as W increases, which is against the experimental results in Fig.5. In ethylenediamine solution, silicon is etched through two reaction steps. First the $Si(OH)_6^{2-}$ compound is formed on the Si surface, then it is dissolved in etylenediamine solution. The latter is a slower reaction, and it rules the etching rate[8]. In the selective polishing, the compound is directly polished off by the polishing pad [9], and the polishing rate Rsi.a depends directly on both W and Rot. From the results in Section 5, however , we concludes that the SOI thickness in a 30μm pattern decreases mainly due to Si etching reaction described above. When the oxide stopper is exposed, the pad can't reach the SOI surface because of a slight step between the SOI and the stopper.

As the pattern size increases, dishing effect would become larger, and it would rule the SOI thickness decrease at last. In order to find the limit size, Rsoi dependence on the SOI pattern size is measured as shown in Fig.8. The dependence of Si etch rate in ethylenediamine solution is also shown in the same figure. All data are normalized by the rate in a 50 μm pattern.

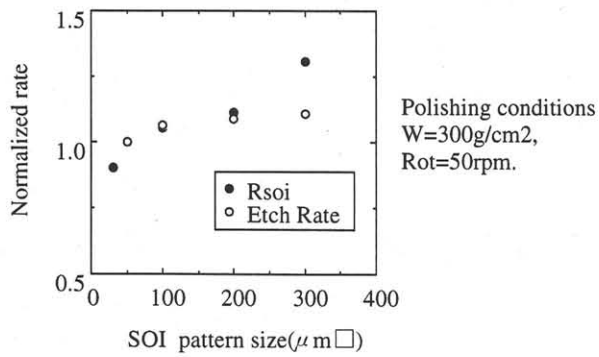


Fig.8. Rsoi dependence on the pattern size

Both dependencies of Rsoi and Si etch rate are the same where the pattern size is less than 200 μm. The difference between them appears at the pattern size of 300 μm. The limit size exists at between 200 and 300 μm.

The etching rate Rsoi depends only on the pad temperature T as shown in Fig.7. Neither W nor Rot has direct influence on Rsoi. However they affect Rsoi indirectly through increase of the pad surface temperature (T), which increases proportionally to W and Rot.

As described above, the dependence of Rsoi on W or Rot, is different from that of Rsi.a. Using this difference, we can increase the selectivity with optimizing W and Rot.

7. Decreasing Δ Tsoi

3 bonded wafers having Tsi.a=3 ~ 4 μm and ΔTsi ~ $\pm$ 0.6μ m were prepared. After 0.5 μm chemical mechanical polishing, the selective polishing was performed at the pressure=300g/cm2, the rotation speed=30,50,70rpm with the ultra flat porous chuck. The SOI thickness in a 30μm square pattern was evaluated across the 8-inch wafer (for 76 available chips). 30 μm square SOI patterns in 91,97,95% of the available chips were controlled to within 100$\pm$15nm thickness for the rotation speed condition of 30,50,70rpm respectively. The SOI thickness distribution for the rotation condition of 50rpm, is shown in Fig.9.

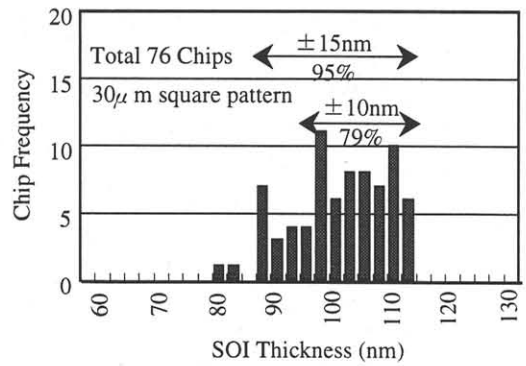


Fig.9. SOI thickness uniformity in an 8-inch wafer

8. Summary

A bonded SOI process with a selective polishing was improved for an 8-inch wafer fabrication. The process fluctuations disturbing the SOI thickness uniformity were reduced for both grinding and polishing. The polishing selectivity was improved by optimizing pressure and rotation speed conditions. Consequently a 100 $\pm$15nm thick SOI wafer was successfully obtained.

9. Acknowlegement

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