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Enhancement and Suppression of Band-to-Band Tunneling Current in Ultra-Thin nMOSFETs/SIMOX: Influence of Superficial Si Layer Thickness and It's Future Prospect

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The significant features of band-to-band tunneling (BBT) current characteristics in extremely-thin SOI devices are discussed. The BBT current increases with decreasing superficial Si layer thickness. The increase in $E_g(2D)$ caused by the quantum mechanical effect suppresses the BBT current in an extremely-thin Si layer. Considering the quasi constant voltage scaling law, the BBT current takes the maximum at $t_{Si} \approx 5$ nm, and I_{BBT} is reduced when t_{Si} is less than 5 nm, even though, according to the scaling law, the surface electric field increases.

1. INTRODUCTION

Ultra-thin fully-depleted SOI devices are possible candidates for future VLSIs. A low leakage current is required for low-voltage, low-power operation of these devices. The band-to-band tunneling (BBT) current is one type of leakage current.[1),2)] Although the suppression of BBT current is important, the BBT current characteristics for ultra-thin SOI devices are still unclear.

This paper describes the significant features of BBT current characteristics in extremely-thin SOI devices. The characteristics are discussed focusing on the influence of the superficial Si layer thickness and the explicit quantum mechanical effect. The experimental data is interpreted with the aid of two-dimensional device simulations. The BBT current characteristics are also discussed for a device miniaturized according to the scaling law.

2. EXPERIMENTAL

A buried-channel nMOSFET device with a 10-nm-thick gate oxide and 10-μm-long gate was fabricated on a SIMOX substrate with a 100-nm-thick buried oxide layer. Two superficial Si layer thicknesses (t_{Si}), 7.5 and 50 nm, were prepared. In the case of $t_{Si} = 7.5$ nm, a recessed gate structure was employed to avoid the parasitic resistance problem (Fig. 1). The superficial Si layer thickness was measured with a spectroscopic ellipsometer and a step analyzer (Alpha step-200). The n-type body had a doping concentration (N_D) of 1×10^{17} cm^{-3}. The designed doping concentration of the n-type source and drain regions was 6×10^{20} cm^{-3} and these regions were annealed at 900 °C for 15 min. The off-state drain current at the gate voltage (V_G) of -2 V was measured with no substrate bias. The gate was long enough to restrain the parasitic bipolar effect.

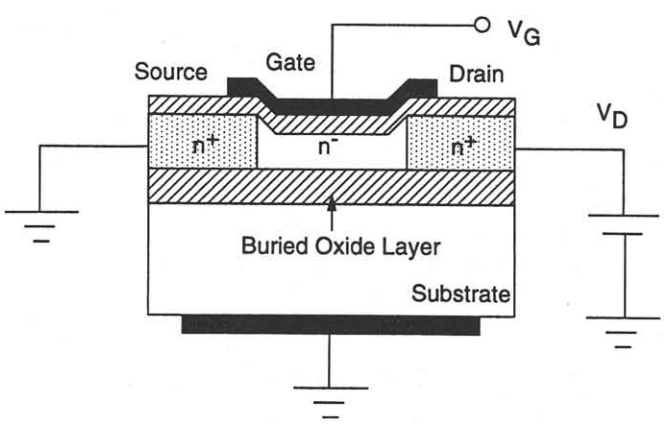

Fig. 1 The recessed gate device structure for the buried-channel nMOSFET/SIMOX in the case of $t_{Si} = 7.5$ nm.

3. RESULTS AND DISCUSSIONS

The drain current (I_D) dependence on drain voltage (V_D) in buried-channel nMOSFETs/SIMOX is shown in

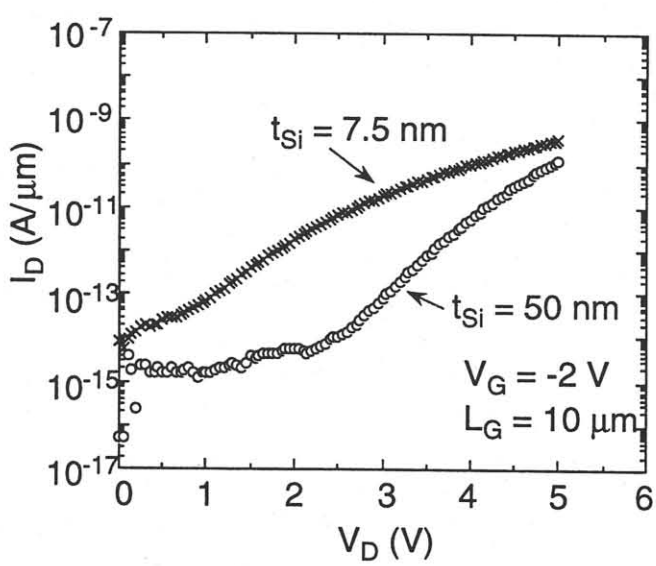

Fig. 2 Drain current characteristics of MOSFETs/SIMOX with $V_G = -2$ V, $L_G = 10$ μm, and $t_{Si} = 7.5$, 50 nm.

Fig. 2 for the two superficial Si layer thicknesses (t_{Si})[3]. I_D increases with decreasing t_{Si}. From the simultaneous measurement of gate current, it was confirmed that I_D mainly consists of BBT current (I_{BBT}). Similar drain current characteristics were also observed in pMOS devices.

I_{BBT} is a function of surface electric field (E_s) and is represented theoretically as

$$I_{BBT} = A\, E_s \exp(-B/E_s), \qquad (1)$$

where A and B are constants.[2)~6)] E_s at the SiO_2 / Si interface in the drain region was simulated with a two-dimensional (2-D) device simulator. The electric field distribution in the SOI device is plotted in Fig. 3. The electric field takes the maximum value at the edge of the drain region, so band-to-band tunneling occurs in the gate-to-drain overlap region.[2)]

The maximum simulated value of electric field at the drain edge is plotted against t_{Si} in Fig. 4. This result suggests that the maximum electric field increases with decreasing t_{Si}. This feature holds independently of the drain voltage and the gate length.

The previous discussion leads to another consideration; BBT current characteristics can be anticipated when the superficial Si layer becomes extremely thin. However, the explicit quantum mechanical effect must be taken into account in the 2-D Si structure. Parameter B is expressed as a function of bandgap energy (E_g) according to

$$B = (\pi m^{*1/2} E_g^{3/2})/2q\hbar, \qquad (2)$$

where m^* is the effective mass of electrons and q is the elementary charge.[1)] Equation (2) suggests that B increases with increasing E_g. Figure 5 is a schematic band diagram of an SOI structure whose superficial Si layer is thinned down to less than 10 nm.[7)] Since the superficial Si layer is thin enough for 2-D quantization, individual sub-band energy levels are manifested. The effective bandgap energy in the 2-D system, $E_g(2D)$, can be estimated by an effective-mass approximation and assuming the infinite confining potential of SiO_2 as

$$E_g(2D) = E_g(3D) + \Delta$$
$$= E_{n,1} - E_{p,1}\ , \qquad (3)$$

where Δ is the energy difference, $E_{n,1}$ is the lowest level of sub-band level for electrons and $E_{p,1}$ is that for holes. Figure 5 and eq. (3) indicate that E_g increases when t_{Si} becomes extremely thin.

The BBT current can be calculated for the

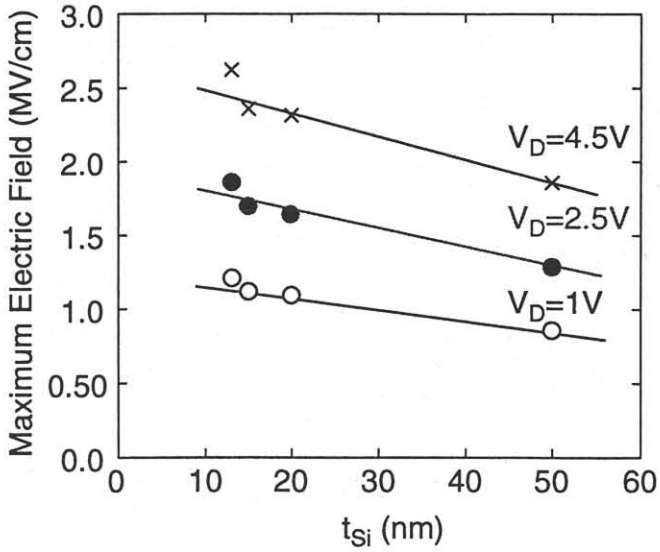

Fig. 4 Simulated maximum surface electric field at the SiO_2 / Si interface in the drain region for V_G = -2 V, L_G = 2 μm. The drain voltage was set at 1, 2.5 or 4.5 V.

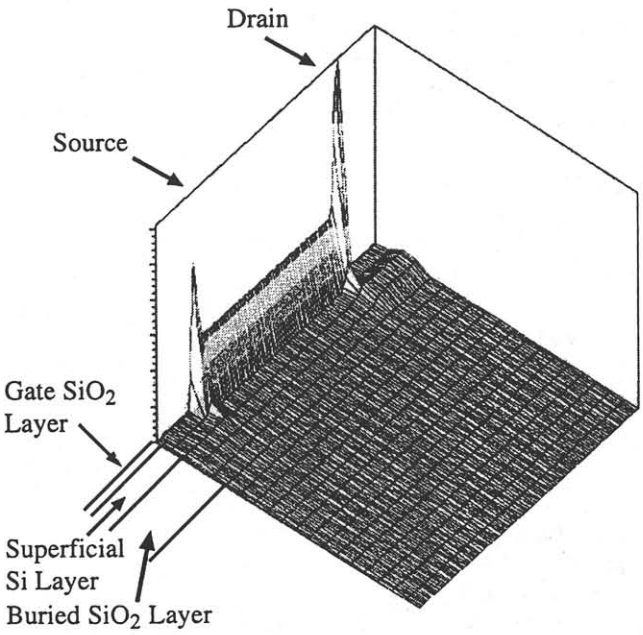

Fig. 3 Electric field distribution in the superficial Si layer with V_D = 1 V, V_G = -2 V, L_G = 2 μm, and t_{Si} = 50 nm.

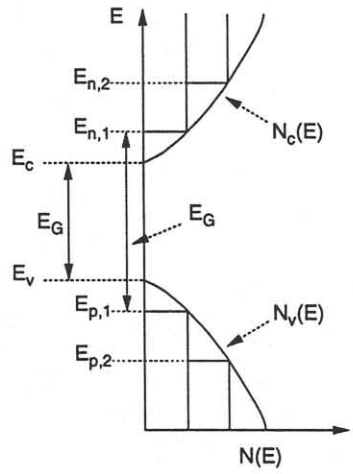

Fig. 5 Schematic band diagram of an SOI structure whose superficial Si layer is thinned down to less than 10 nm.

Table 1
Definitions of scaling laws[8)]

Scaling law	Constant Field	Constant Voltage	Quasi Constant Voltage
General Dimensions	1/k	1/k	1/k
Gate Oxide Thickness	1/k	$1/\sqrt{k}$	1/k
Doping Conc.	1/k	1/k	1/k
Voltage	1/k	1	$1/\sqrt{k}$

superficial Si layer thickness using eqs. (1), (2), and (3). We assume that E_s increases monotonically when the superficial Si layer is less than 10 nm. Other device parameters are fixed. In this case, it is found that the calculated BBT current increases with decreasing t_{Si}, and that it takes the maximum at $t_{Si} \approx 10$ nm. The BBT current is reduced when the superficial Si layer is less than 10 nm, in spite of increasing E_s. The increase of $E_g(2D)$ suppresses the BBT current of extremely-thin SOI device.

In a practical situation, not only t_{Si} but also other device parameters are scaled down in accordance with the scaling law for extremely-thin SOI devices. The whole effect of device parameters must be considered in any discussion of the BBT current characteristics.

Three scaling laws are shown in Table 1.[8)] A quasi constant voltage scaling law was used in this work, which is representative of trends in device scaling. According to this scaling law, the scaling scheme is defined with 1/k for gate oxide thickness (t_{ox}) and t_{Si} and with $1/\sqrt{k}$ for supply voltage (V_{DG}). Down-scaling of t_{ox} and V_{DG} results in an increase in E_s by $\sqrt{k}$, which was also confirmed by the empirical surface field equation using T. Y. Chan's form:[2)]

$$E_s = (V_{DG} - 1.2)/(3t_{ox}) . \qquad (4)$$

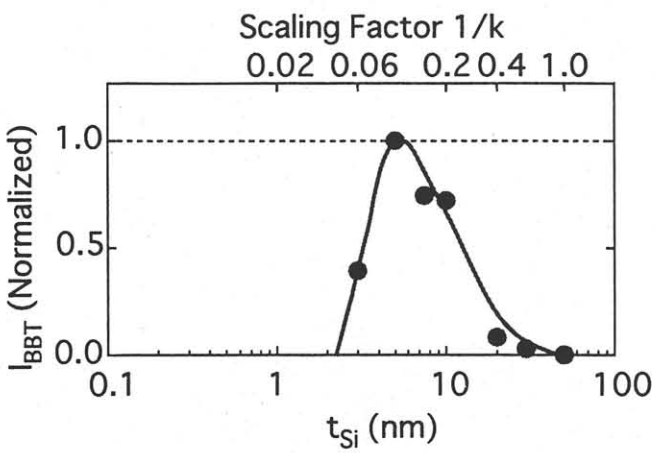

Fig. 6 The calculated I_{BBT} dependence on t_{Si}. I_{BBT} is normalized at the maximum value. Scaling factor k is normalized for $t_{Si} = 50$ nm.

The I_{BBT} dependence on t_{Si} calculated using eqs. (1), (2), and (3) is shown in Fig. 6. Device parameters such as V_{DG}, t_{Si}, t_{ox} are changed according to the device road map,[9)] which is governed by the quasi constant voltage law. Scaling factor k is normalized for $t_{Si} = 50$ nm. I_{BBT} is normalized at the maximum value. I_{BBT} increases with decreasing t_{Si}, and it takes the maximum at $t_{Si} \approx 5$ nm. Since the electric field in the superficial Si layer increases relatively in the quasi constant voltage scaling law, the maximum position shifts to 5 nm. In this region, I_{BBT} is reduced when t_{Si} is less than 5 nm. The effective band gap energy suppresses I_{BBT}, even though E_s increases by $\sqrt{k}$. Therefore, the BBT current is suppressed in extremely-thin SOI devices.

4. SUMMARY

The significant features of BBT current characteristics in extremely-thin SOI devices have been discussed. The BBT current increases with decreasing superficial Si layer thickness. Simulation results suggest that the surface electric field increases with decreasing superficial Si layer thickness, which leads to the increase in BBT current.

Also discussed were the BBT current characteristics when the superficial Si layer becomes extremely thin. The explicit quantum mechanical effect appears in the 2-D Si structure. The increase in $E_g(2D)$ suppresses the BBT current in an extremely-thin Si layer. Considering the quasi constant voltage scaling law, the BBT current takes the maximum at $t_{Si} \approx 5$ nm, and I_{BBT} is reduced when t_{Si} is less than 5 nm, even though the surface electric field increases according to the scaling law. This will be a significant advantage for future SOI devices.

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