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Impact of Current Gain Increment Effect on Alpha Particle Induced Soft Errors in SOI DRAMs

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We examined alpha particle induced charge in the SOI DRAMs where lifetime of minority carriers is relatively long. We found that collected charge in SOI DRAM with an n-type gate is larger than in SOI DRAM with a p-type gate. The difference in the work function between the gate and the body results in a significant increase in current gain. It is necessary to consider the effect of current gain increment in SOI DRAM design.

1. Introduction

Alpha particles emitted by radioactive impurities in chip packaging materials can cause soft errors in DRAMs [1]. Ever since this was discovered, the problem of soft errors induced by alpha particles has been extensively studied. A silicon-on-insulator (SOI) DRAM is capable of suppressing charge collected due to the funneling and diffusion phenomena. For example, the collected charge at the bit line of the SOI DRAM is smaller than the detection limit [2].

The floating body effects must be considered in the examination of SOI DRAMs. When an alpha particle hits the body region of an SOI DRAM, the generated electrons immediately drift into the source or the drain region, while the remaining holes raises the body potential. As a result, the source-body junction becomes forward-biased. Also, extra electrons are injected from the source region, which connects the bit line, and collected at the drain region, which connects the cell capacitance. This is called the bipolar effect [3]. In the bipolar effect, more charge is collected at the cell capacitance than is generated in the body region.

The lifetime of minority carriers in SOI MOSFET is shorter than in bulk MOSFET [4]. When the lifetime of minority carriers is short, the leakage current at the drain is large, which means deterioration of charge retention of the cell capacitance. Therefore, long minority-carrier lifetime is desired for reliable DRAM.

Since such DRAMs have not been available until now, the bipolar effect has not been examined for SOI DRAMs where the lifetime of minority carriers is relatively long. The purpose of this paper is to examine the resistance of SOI DRAMs with a sufficiently long minority-carrier lifetime against soft error.

2. Current Gain Increment Effect

Using a three-dimensional device simulator [5], we examined collected charge in a typical SOI DRAM (Fig. 1). We focused on a partially depleted SOI MOSFET, which is more realistic than a fully depleted SOI. We concentrated on a long channel SOI MOSFET for clarifying the bipolar effect in the absence of short channel effect. In analyzing the bipolar effect, it is important to consider the transient body potential that depends on the voltage variation of the bit line or word line. Here, we have assumed that the body region is in thermal equilibrium with the source region before an alpha particle incidence. We also assumed that the drain voltage is constant, although it varies with the charge collected at the cell capacitance in reality.

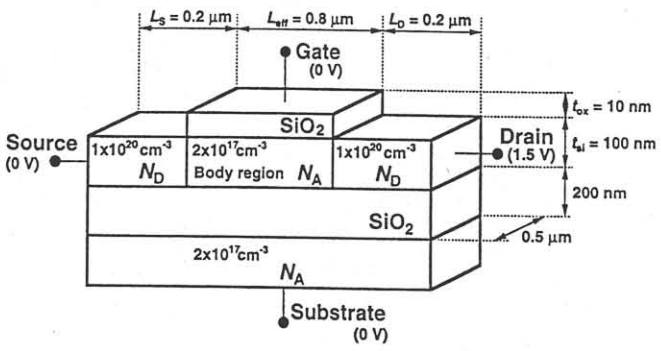

Fig.1 The SOI MOSFET structure used in this study. A 2-MeV alpha particle passes though the center of the body region, and it is normal to the SOI surface. The generated charge (Q_i) in the body region is about 1.06 fC.

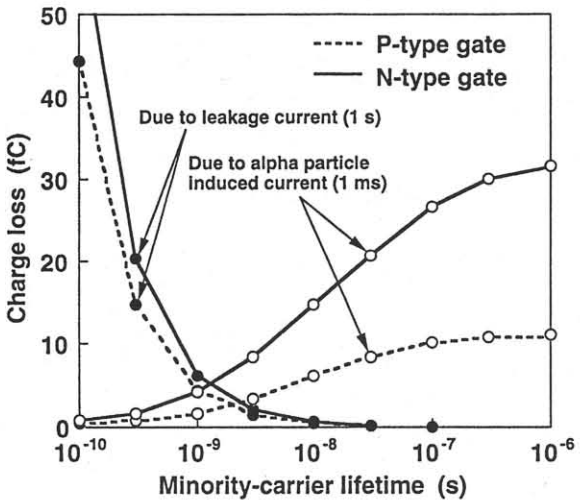

Fig.2 The dependency of charge loss at the drain terminal on minority-carrier lifetime.

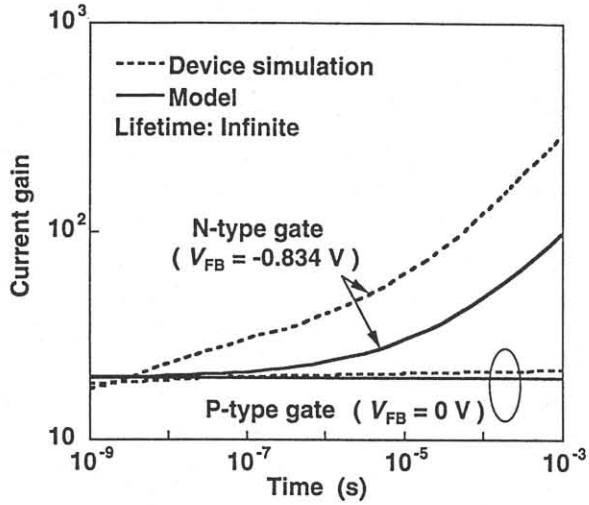

Fig.3 Current gain of SOI DRAMs with p-type and n-type gates. We assumed an infinite minority-carrier lifetime here.

We examined the dependency of charge loss on the lifetime of minority carriers (Fig. 2). To simplify the estimation of surface recombination velocity, we assumed that the minority-carrier lifetime is constant in the silicon layer. A minority-carrier lifetime of 20 ns corresponds to a surface recombination velocity of 250 cm/s in an SOI of 100 nm in thickness, which is the typical surface recombination velocity in SOI MOSFET [4]. Although charge loss due to current leakage in 1 sec decreased as the minority-carrier lifetime increased as expected, the alpha particle induced charge in 1 ms increased (Fig. 2) on the other hand. When the minority-carrier lifetime is short enough, the generated holes recombines with the electrons around the body-source junction. This suppresses the bipolar effect, and the collected charge decreases. The soft error rate obtained from a SOI DRAM with short minority-carrier lifetime is different from the rate obtained from one with longer minority-carrier lifetime. Therefore, it is important to evaluate resistance against soft error using SOI DRAMs with longer minority-carrier lifetime.

We discovered that, when the lifetime of minority carriers is long, the collected charge in an SOI DRAM with an n-type gate is larger than in one with a p-type gate (fig. 2). The broken lines in Figure 3 show variation of current gain with time, where the current gain is defined as the ratio of electron current to hole current at the source terminal. Although the current gain is assumed to be constant with respect to time in conventional works [6], the current gain obtained with an n-type gate started increasing before the refresh whose interval is typically from 10 ms to 100 ms. Although the collected charge after 1 ms could not be obtained with our simulator due to a convergence problem, the collected charge during the refresh period should become relatively large when the minority-carrier lifetime is long enough for an n-type gate.

3. Current Gain Increment Mechanism

To understand the current gain increment observed in the simulation, we derived an analytical expression for current gain. Figure 4 and Figure 5 show the vertical band diagram near the source-body junction for a p-type gate and for an n-type gate when the body potential rises to V_{body}. We obtained electron concentration in the body region as a function of body potential by solving the Poisson equation analytically. The electron injection current can be calculated using the electron concentration. The current gain then can be estimated from the ratio of electron injection current to hole current:

$$h_{FE}(t) = h_{FE0}\left[1+\frac{W_{dep}(t)}{2t_{si}}\left[\frac{V_t}{\psi_s(t)-V_{body}(t)}\left[\exp\left(\frac{\psi_s(t)-V_{body}(t)}{V_t}\right)-1\right]-1\right]\right],$$

where,

$$\psi_s(t) = \begin{cases} -V_{FB}+V_0-\sqrt{V_0^2-2V_0\left(V_{FB}+V_{body}(t)\right)} & \text{for } V_{body}(t) \le -V_{FB} \\ V_{body}(t) & \text{for } V_{body}(t) > -V_{FB} \end{cases},$$

$$I_h(t) = I_s\left[\exp\left(V_{body}(t)/V_t\right)-1\right] = \frac{Q_0}{t+Q_0/I_{h(0)}},$$

$$W_{dep}(t) = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}\left(\psi_s(t)-V_{body}(t)\right)}{qN_A}}, \quad h_{FE0} = \frac{D_n}{D_p}\frac{L_s}{L_{eff}}\frac{n_{p0}}{p_{n0}},$$

$$V_t \equiv \frac{kT}{q}, \quad V_{body}(0) = \frac{Q_i}{C_{gate}}, \quad V_0 \equiv \frac{q\varepsilon_0\varepsilon_{si}N_A t_{ox}^2}{\varepsilon_0^2\varepsilon_{ox}^2}, \quad Q_0 \equiv C_{gate}V_t,$$

$$n_{p0} = \frac{n_i^2}{N_A}\exp\left(\Delta E_{gB}/kT\right), \quad p_{n0} = \frac{n_i^2}{N_D}\exp\left(\Delta E_{gS}/kT\right).$$

We compared the current gain of our model with the results obtained in device simulation (Fig. 3). When the flat-band voltage (V_{FB}) is zero (Fig. 4), the current gain is independent of time in our model. This agrees with the

results of device simulation. When the flat-band voltage is negative (Fig. 5), the electron potential at the front interface is lower than at the back interface. Electrons are injected in the region around the front interface from the source region, while holes are injected in the source region from the flat band region in the body. This means that the electron barrier height (ϕ_n) is lower than the hole barrier height (ϕ_p). As the body potential drops due to hole injection in the source region, the difference between the electron barrier and the hole barrier (ϕ_p - ϕ_n) increases. This implies that current gain increases with time. This current gain increment also agrees with the results of device simulation (Fig. 3). Therefore, when the vertical band in the body region bends at a steady-state, current gain increment occurs and the collected charge increases significantly.

4. Discussions

The use of a wide-gap material in the source region is effective in decreasing current gain [6]. However, when the vertical band in the body region bends, the current gain will also increase with time after an alpha particle passes through the body region. Therefore, the collected charge, taking the current gain increment effect into account, needs to be estimated for further understanding and hopefully preventing soft error even in devices with a wide-gap source region.

A flat vertical band in the body region is desired to reduce collected charge. Although a p-type gate material furnishes the flat-band condition, the accompanying threshold voltage is too high. We should therefore design a device structure that simultaneously satisfies the flat-band requirement and produces a suitable threshold voltage; otherwise, SOI DRAMs with reliable charge retention and soft-error resistance will not be practicable.

5. Summary

We investigated collected charge in SOI DRAMs where minority carriers are a sufficiently long lifetime. We found that, when the minority carrier lifetime is long, the collected charge in an SOI DRAM with an n-type gate is larger than in one with a p-type gate material. The difference in the work function between the gate and the body results in a significant increase in current gain. We need to develop a device structure that simultaneously satisfies the flat-band requirement and produces a suitable threshold voltage.

References

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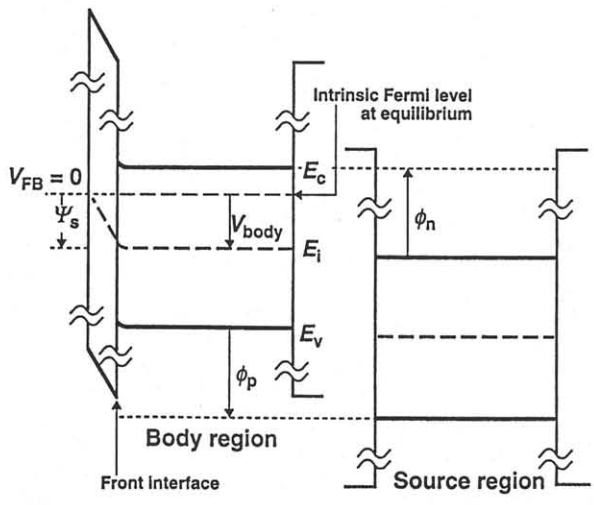

Fig.4 Schematic vertical band diagram for a p-type gate. The height of electron barrier (ϕ_n) equals the hole barrier height (ϕ_p); the relationship is independent of the body potential.

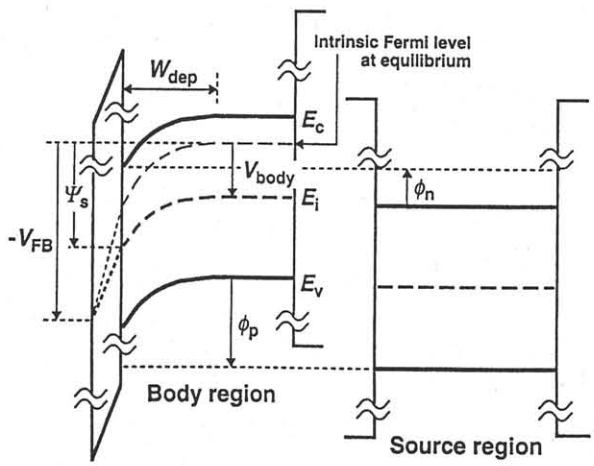

Fig.5 Schematic vertical band diagram for an n-type gate. V_{FB} is the flat-band voltage and is a negative value. The electron barrier height (ϕ_n) is lower than the hole barrier height (ϕ_p).