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Analysis on the Threshold Voltage Fixing and the Floating-Body-Effect Suppression for 0.1 μm Fully Depleted SOI-MOSFET

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Abstract: Threshold voltage (V_{th}) adjustment for 0.1μm fully depleted SOI-MOSFET, is analyzed as a two dimensional problem on the electric field between the acceptor ion and the electrodes of SOI-MOSFET, using device simulation and a simple analytical model (capacitance net work model). The dopant concentration required to compensate the two dimensional effect for the V_{th} adjustment is derived. Moreover, an offset narrow gap source structure is proposed, in order to suppress the floating body effect which is enhanced when the acceptor concentration increases for V_{th} adjustment.

1.Introduction

For a 0.1 μm SOI-MOSFET, the electrostatic coupling between the channel region and S/D increases, and this coupling approaches to that between the channel and the gate electrode[1]. This paper reports the doping optimization for the V_{th} adjustment, which is required to compensate the influence of the coupling between the channel and S/D. The floating body effect suppression by compensating an enhancement on this effect due to the increased dopant concentration for the V_{th} adjustment, is also reported.

2.On V_{th} degradation

The potential distribution is calculated by combining capacitance networks between the electrodes and the channel[1](Fig.1a) and that between the acceptor ion and the electrodes(Fig.1b). The potential of the SOI body, ϕ , is given by a simple equation as in Eq.1(Table.1). The result (Solid lines in Fig.2) agrees with the numerical simulation (broken lines). The ratio R_{field}, which is a ratio of the vertical electric field caused by the acceptor ions for the short channel device (E_{vert}) and that for the long channel device (E_{long}), is given by Eq.6(Fig.3). The result agrees with the simulation. R_{field} degrades as the gate length decreases or the SOI thickness increases. The reason is that the electrostatic coupling between the acceptor ion and S/D (C_{cs} and C_{cd} in Fig.1b) increases, and consequently the coupling with the gate electrode decreases. Fig.3 indicates that the doping for V_{th} adjustment should be increased in order to compensate the degradation of electric field, when the gate length issmall or the SOI thickness is large. The ratio R_{Vdrop}, which is a ratio of the acceptor induced vertical potential drop across the SOI body for the short channel device (V_{vert}) and that for the long channel device (V_{long}), is given by Eq.7(Fig.4). The degradation of R_{Vdrop} is larger than R_{field}. Therefore, an increase in R_{Vdrop} due to the increased dopant concentration for the V_{th} adjustment, is smaller then that in R_{field}. This result indicates that the full depletion can be achieved even when the dopant concentration is increased, since the partial depletion is achieved when the vertical potential drop across the SOI layer is large. The acceptor concentration required to V_{th} adjustment is given by Eq.8(Fig.5), by considering the above result and the contribution of the S/D induced electric field at the channel (Fig.1a). The lines are plotted for the condition where the full depletion is achieved while still keeping the back channel suppressed at the threshold voltage.

By introducing shallow S/D extension (Structure.1 in fig.6), the vertical electric field is regained(Open circles in figs.3 and 4), since the capacitance between the acceptor and the S/D decreases. The acceptor concentration required for this device is low(5×10^{17}cm^{-3}), for V_{th}=0.25V at V_D=1.4V, L=0.1μm and T_{SOI}=500Å.

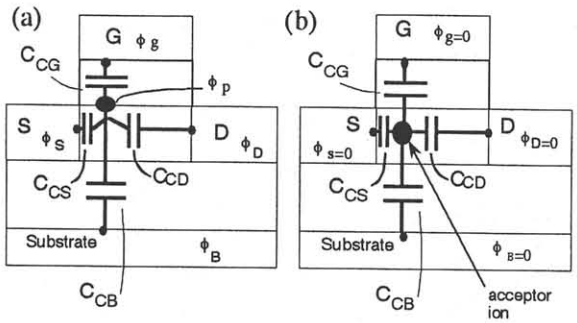

Figure.1. The capacitance network model. (a) for the elecrtric field due to the potential of the electrodes,(b) for the electric field from the acceptor ions. The potenital of the electordes in (b) is assumed to be zero.

3.On floating body effect

When a vertical electric field required for V_{th} adjustment is achieved, the onset drain voltage for the floating-body-effect decrease, since the vertical electric field produces a low potential region in the SOI layer where the hole concentration increases. Therefore, for a rather high applied voltage (>1.4V), the floating body effect suppression should be linked to the V_{th} control. Structure.2 in fig.6 shows a new structure for the narrow gap source[2] SOI-MOSFET. In this device, the narrow gap material is placed off-set from the source junction. This off-set structure avoids the saturation in the diffusion current (hole current) at the ON region (where E_{Fp} is small, in Fig.9b). This saturation is caused by a barrier for the hole diffusion, which is located at the hetero junction(Fig.8). This barrier is significant at the ON region, where the potential of the body increases, since E_v at the hetero junction becomes low. In the structure 2, the narrow gap region ($Si_{0.5}Ge_{0.5}$) is extended to the p$^-$ region under the S/D extension area, and the hetero junction is placed off-set from the tip of the S/D extension. Therefore, the potential of the hetero junction is not affected by the channel potential, and the barrier for the hole diffusion is suppressed even for the ON region (the band diagram shown by broken line in Fig.8). Moreover, the hole accumulation at the narrow gap region (due to high E_v[3]) does not affect the channel, since it is off-set from the channel region, and the electric field at the hetero junction, where the crystal quality tends to be bad, is also decreased (this effect is important when the device have symmetrical narrow gap regions at the source and the drain). This structure is designed by assuming fabrication processes such as the lateral epitaxial growth of SiGe, or Ge implantation to SOI layer. The simulation result on this structure indicates that the floating body effect does not occurs for V_D=2.2V, and that S=84mV/dec. for T_{ox}=50Å(Fig.7), 74mV/dec. for T_{ox} = 30A can be achieved.

4.Conclusion

The V_{th} retention for 0.1μm SOI-MOSFET is analyzed using a simple capacitance network model. The model agrees with the simulation. An expression to estimate the doping concentration is obtained using this model. A new device structure with off-set narrow gap source is proposed. The simulation result shows that this device has a good V_{th} controllability, low S factor, and floating-body-effect tolerance in the 0.1μm region, while still keeping the advantages of SOI-MOSFET such as low parasitic capacitance and body effect free characteristics.

References

[1]R.Koh et.al, Ext. Abs. 1996SSDM, p.863
[2]M.Yoshimi et.al, IEDM'94, p.429
[3]O.Arisumi et.al, Ext. Abs. 1996SSDM, p.860

Table 1

$$\phi_p = (C_{cg}\phi_g + C_{cs}\phi_s + C_{cd}\phi_d + C_{cb}\phi_b) / (C_{cg} + C_{cs} + C_{cd} + C_{cb})$$
$$- R_{field} T_{SOI} q N_A T_{OX}/\varepsilon_0\varepsilon_{ox} - R_{Vdrop} q N_A (2yT_{SOI} - y^2)/ 2\varepsilon_0\varepsilon_{si} \quad (1)$$

$$C_{cg} = \varepsilon_0 \varepsilon_{ox} / (T_{ox} + y(\varepsilon_{ox} / \varepsilon_{si})) \quad (2)$$

$$C_{cb} = \varepsilon_0 \varepsilon_{ox} / (T_{box} + (T_{SOI} - y) \varepsilon_{ox}/ \varepsilon_{si}) \quad (3)$$

$$C_{cs} = \varepsilon_0 \varepsilon_{Si} (1 + y^2/a_1^2)(T_{SOI} + b) / (x^2 + cx) \quad (4)$$

$$C_{cd} = \varepsilon_0 \varepsilon_{si} (1 + y^2/a_1^2)(T_{SOI} + b)/ ((L - x)^2 + c (L - x)) \quad (5)$$

a_1 = 650Å, b=70Å, c=50Å, y: distance from SOI Surface, x: distance from source, T_{SOI}:SOI Thickness

T_{OX}: gate oxide thickness, T_{box}: burried oxide thickness , N_A : acceptor concentration

$$R_{field} = E_{vert}/E_{long}$$

$$= - \frac{C_{OX}}{q N_A \cdot Tsoi} \int_0^{Tsoi} q \cdot \frac{N_A}{Ccg + Cs + Cd + Cb} \frac{Tox}{Tox + \frac{y \cdot \varepsilon ox}{\varepsilon si}} dy$$

$$= C_{SOI}/ (C_{cs} + C_{cd})$$
$$\times \log [(C_{cs} + C_{cd} + C_{BOX}) C_{ox} / (C_{SOI} C_{ox} + C_{SOI} (C_{cs} + C_{cd} + C_{BOX})\} + 1)] \quad (6)$$

In Eq.6 C_{cb} is approximated by a constant C_{BOX} ($= \varepsilon_0 \varepsilon_{Si}/T_{box}$). By an approximation assuming acceptors concentrate at $y=T_{SOI}/2$, Eq.6 becomes Eq.6'.

$$R_{field} = C_{cg}' / (C_{cs} + C_{cd} + C_{cb}' + C_{cg}') \quad (6')$$

$$C_{cg} = \varepsilon_0 \varepsilon_{ox} / (T_{ox} + (T_{SOI}/2) (\varepsilon_{ox} / \varepsilon_{si})), \quad C_{cb} = \varepsilon_0 \varepsilon_{ox} / \{T_{box} + (T_{SOI} / 2) (\varepsilon_{ox}/ 2 \varepsilon_{si}) \}$$

$$R_{Vdrop} = V_{vert}/V_{long} = R_{field}\{1- (C_{cb} + C_{cs}/\delta + C_{cd}/\delta) / C_{SOIB}\} \quad (7)$$

$C_{OX} = \varepsilon_0 \varepsilon_{ox}/T_{OX}$, $C_{SOI} = \varepsilon_0 \varepsilon_{Si}/T_{SOI}$, $C_{SOIB} = \varepsilon_0 \varepsilon_{Si}/(T_{SOI}-y)$

δ: Fitting parameter to include the 2D electric field profile under the acceptor ion (=1.7).

$$N_A = (C_{OX} / R_{field})\{-\phi_{inv}+(C_{cg}V_{th}+C_{cs}\phi_s+C_{cd}\phi_d+C_{cb}\phi_b)/ (C_{cg}+C_{cs}+C_{cd}+C_{cb})\}/ qT_{SOI} \quad (8)$$

ϕ_{inv}:Inversion potential (-0.14V)

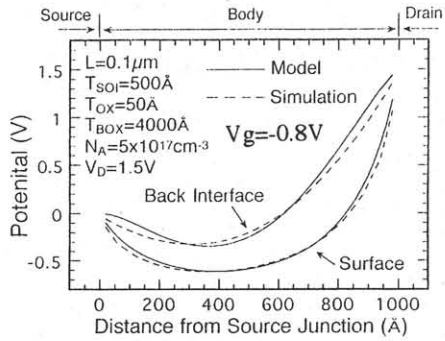

Figure.2 The potential distribution for SOI surface and back interface. The broken lines indicate the result for simulation, and the solid line for the model.

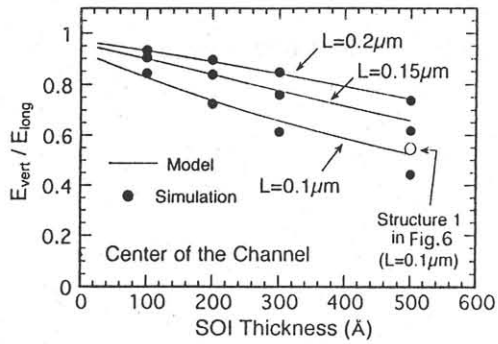

Figure3. The ratio of the vertical electric field,short channel device to the long channel device (R_{field}).

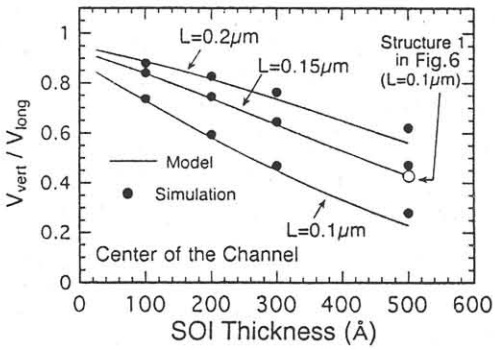

Figure4. The ratio of the vertical potential difference in the SOI layer, short channel device to the long channel device (R_{vdrop}).

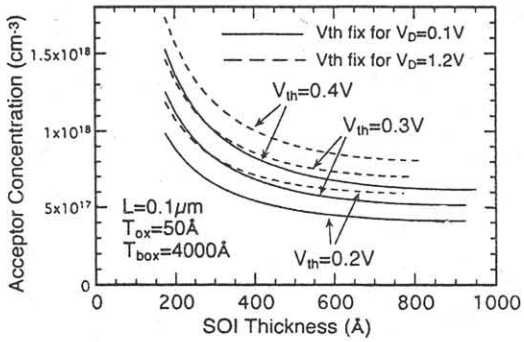

Figure 5. The acceptor concentration required to fix V_{th} .

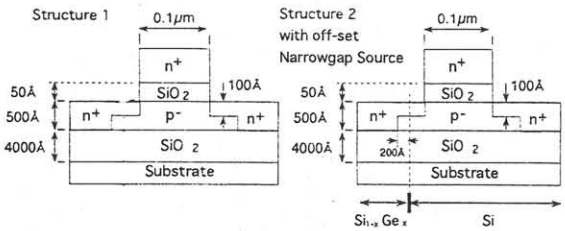

Figure6. Structure.1 : a structure having S/D extention. Structure.2: a structure with off-set narrow gap source.

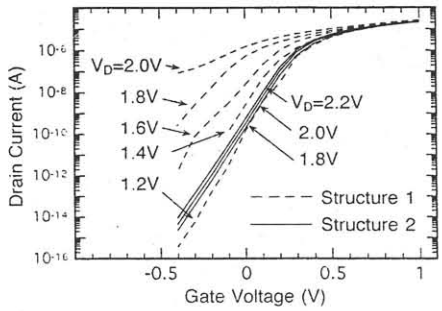

Figure7. The subthreshold characteristics of Structure.2 in Fig.6(Solid line). Broken lines show that for Structure.1 where narrow gap material is not used, where the abnormal operation increases the subthreshold current for Vd > 1.4V.

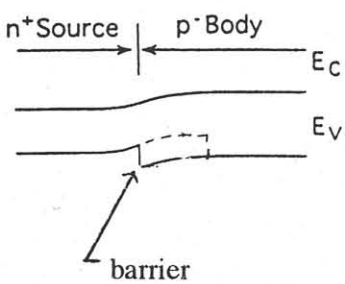

Figure8. The potential barrier for the hole diffusion, formed around the threshold voltage. The broken line shows the off-set narrow gap structure.

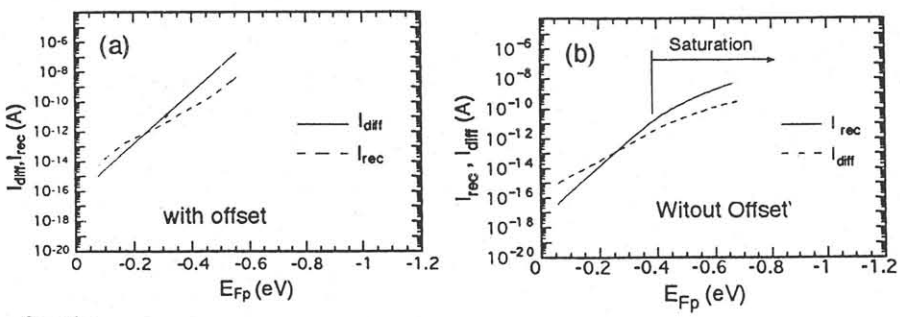

Figure 9. The diffusion (I_{diff}) and reccombination (I_{rec})) current for (a) with off-set narrow gap source without , (b) narrow gap source without off-set (pn junction corresponds to hetero junction).