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Effect of ECR CVD SiO_2 Film Deposition on Ferroelectric Properties of Pt/PZT/Pt Capacitor

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The influences of ECR CVD SiO_2 layer on ferroelectric properties of Pt/PZT/Pt capacitor were investigated. The increases of stress, deposition temperature, and thickness of SiO_2 layer induced the degradation of Pt/PZT/Pt capacitor. When the SiO_2 with the thicknesss of 15000 Å was deposited at the temperature of 200℃ by using ECR CVD, it had the low stress of compressive 3×10^9 dyne/cm^2. The nonvolatile polarization of Pt/PZT/Pt capacitor at the area of $100\times100\,\mu m^2$ was about $9\,\mu C/cm^2$ and could be used as ILD and IMD of double metal FRAM device.

1. Introduction

Recent developments in ferroelectric thin film technology have generated a significant interest for ferroelectric materials in semiconductor memory[1]. Ferroelectric random access memory (FRAM) device has several merits, including the high speed operation, high write endurance and nonvolatility[1]. However, its integration requires several difficult processes in the back-end process after fabricating the $Pb(Zr,Ti)O_3$ (PZT) capacitor; deposition of interlayer dielectric(ILD), metallization, etching and so on. The properties of Pt/PZT/Pt ferroelectric capacitor are very sensitive to those processes. Particularly, the ILD deposition can directly do damage on Pt/PZT/Pt capacitor because it directly contacts Pt/PZT/Pt capacitor. Recently, some researchers have reported the degradation of ferroelectric properties by the ILD process[2]. The ILD film of FRAM using Pt/PZT/Pt capacitor requires the following conditions; low hydrogen concentration, low stress, low thermal budget, and low plasma damage[2]. It is well known that the silicon dioxide deposited by ECR CVD well satisfies these requirements. This paper attempts to investigate the influences of ECR CVD SiO_2 layer on the properties of Pt/PZT/Pt capacitor.

2. Experimentals

We made Pt/PZT/Pt capacitor and compared the ferroelectric properties before and after the ECR CVD SiO_2 deposition. The process flow for this study, shown in Figure 1, is as follow. At first, PZT films with the thickness of 2500 Å were prepared by the conventional sol-gel spin coating method on $Pt/Ti/SiO_2$ (2700/300/1000 Å)[3]. The top electrode Pt with the thickness of 2000 Å was deposited by sputtering. The capacitor with the area of $100\times100\,\mu m^2$ was fabricated by the plasma etching and postannealing under O_2 ambient. The initial measurements such as hysteresis loop, remanent polarization, coercive field, fatigue and leakage current were done by utilizing RT6000S. The maximum applied voltage was 5V and fatigue measurement was done by applying 5V high, $0.5\,\mu$sec wide square wave with 1MHz frequency. TiO_2 barrier layer with the thickness of 300 Å was deposited before the ECR CVD SiO_2 deposition to prevent the interdiffusion between PZT and SiO_2. Then the SiO_2/TiO_2 bilayer was removed by the oxide etchback. Final measurements were done on this capacitor. The effect of ECR CVD SiO_2 deposition was investigated by comparing the initial with final measurement. The investigation parameters were stress, deposition temperature, and thickness of SiO_2 layer. The stress of SiO_2 thin film was calculated from wafer curvature measured using FLEXUS.

3. Results

Hysteresis loops and nonvolatile polarization degradation of Pt/PZT/Pt capacitor with and without the stress of SiO_2 are shown in Figure 2. The nonvolatile polarization was decreased by the compressive stress while the overall shapes of the hysteresis loops were not so much changed by the SiO_2 layer deposition. However, the stress did not change the coercive field and the leakage current, which are ~ 40 kV/cm and $\sim10^{-6}$ A/cm^2 at 5V, respectively. Surprisingly,

the the capacitor stressed by SiO_2 was not so much fatigued after 10^9 cycles and fatigued only a little even after 10^9 cycles in comparison to the unstressed capacitor.

Figure 3 shows the variations of electrical property of Pt/PZT/Pt capacitor, according to the SiO_2 deposition temperature. Although the shapes of the hysteresis loops were changed by the high temperature deposition, the nonvolatile polarization was decreased as the deposition temperature was increased. Particularly the ferroelectric properties of PZT were much degraded and the remanent polarization was dropped below $5\mu C/cm^2$, when the SiO_2 was deposited above 300℃. The fatigue curves were similar to that of Figure 2, except the case at high temperature deposition of SiO_2.

The variations of ferroelectric properties of Pt /PZT/Pt capacitor with respect to SiO_2 thickness are shown in Figure 4. When the SiO_2 thickness was 20000 Å, the effect of SiO_2 thickness on the polarization was much serious. The nonvolatile polarization in the case with 20000 Å thickness was abruptly dropped after 10^9 cycles, while others were similar to that of Figure 2.

In order to cure the ferroelectric properties of Pt/PZT/Pt capacitor degraded by the stress of SiO_2, we annealed the damaged capacitor at 450℃ for 30 min under O_2 ambient, which is shown in Figure 5 and Figure 2(a). When we annealed the capacitor degraded by the stress of -3.5×10^9 dyne/cm^2 (solid line of Figure 5(a)), the hysteresis loop was recovered(dashed line of Figure 5(a)). The post annealing of the capacitor covered by SiO_2 showed the remanent polarization(solid line of Figure 5(b)) comparable to that before SiO_2 deposition. The open circle of Figure 2(b) shows the recovering of the ferroelectric properties of Pt/ PZT/Pt capacitor by the post annealing, too.

It has shown that the ferroelectric properties of Pt/PZT/Pt capacitor is critically dependent on the deposition condition of SiO_2 by using ECR CVD. We may explain those results from the stress of SiO_2 film and the exposure of PZT under H_2 ambient. H_2 ambient can be generated by the decomposition of source gas(SiH_4) during the plasma processing. However, we can overcome those problems, since ECR CVD has a merit of lower temperature processing.

4. Conclusions

We studied the influences of ECR CVD SiO_2 layer on the ferroelectric properties of Pt/PZT/ Pt capacitor. The increases of the stress, deposition temperature, and thickness of SiO_2 layer induced the degradation of Pt/PZT/Pt capacitor, especially nonvolatile polarization. The deposition at the higher temperature than 250℃ caused the severe damage to Pt/PZT/Pt capacitor by the H_2 annealing effect during the deposition, H_2 being generated from the source gas(SiH_4) decomposition during the SiO_2 deposition. ECR CVD SiO_2 with the thickness of 15000 Å which is deposited at the temperature of 200℃ was suitable as ILD and IMD of double metal FRAM device. The nonvolatile polarization of Pt/PZT/Pt capacitor at the area of $100\times100\mu m^2$ was about $9\mu C/cm^2$. The coercive field and leakage current were not changed by the ECR CVD SiO_2 deposition, which were ~ 40 kV/cm and ~ 10^{-6} A/cm^2, respectively.

5. Acknowledgement

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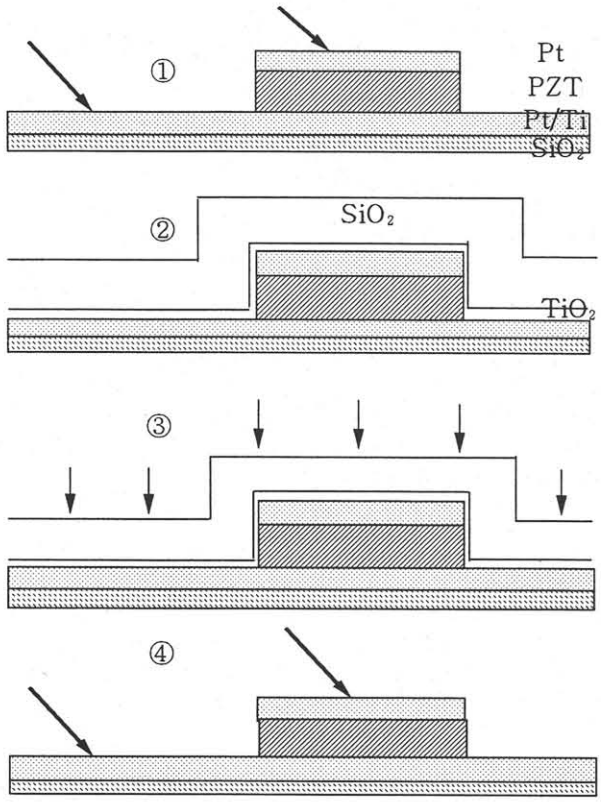
6. References

1) N.Tanabe, et al, VLSI tech Dig., (1995) 123
2) K.Ishihara et al, Integ. Ferro., (1995) 301 ; J.R.Schifko et al, ibid, (1995) 121
3) Y.Nakao et al, ibid, (1995) 23; references therein.



① The fabrication of Pt/PZT/Pt capacitor on Ti/SiO_2 and initial measurement
② SiO_2/TiO_2 deposition
③ etchback of SiO_2/TiO_2 bilayer
④ final measurement

Figure 1. Process flow to investigate the effect of ECR CVD SiO_2 deposition on Pt/PZT/Pt capacitor.

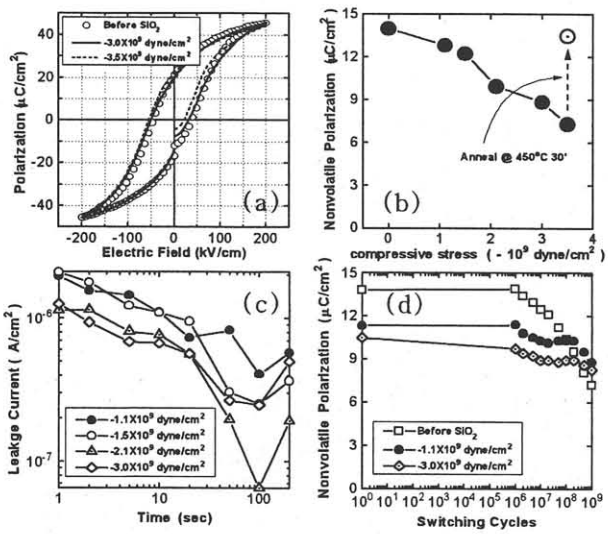


Figure 2. The ferroelectric properties of Pt/PZT/Pt capacitor degraded by the stress of ECR CVD SiO_2; (a) hysteresis loops, (b) nonvolatile polarization, (c) leakage currents and (d) fatigue curves.

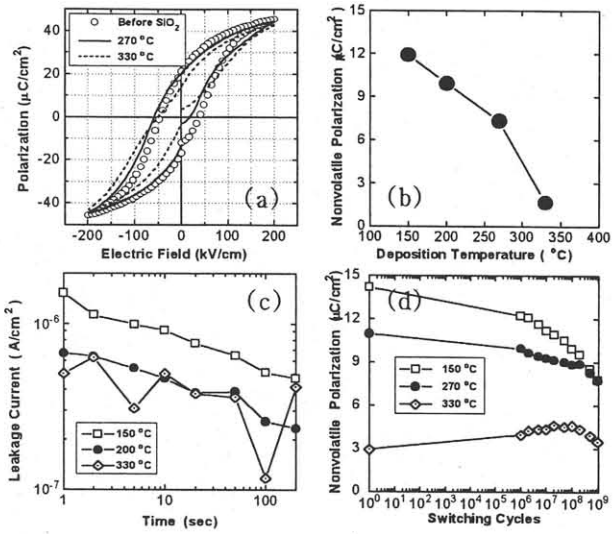


Figure 3. The ferroelectric properties of Pt/PZT/Pt capacitor according to ECR CVD SiO_2 deposition temperature; (a) hysteresis loops, (b) nonvolatile polarization, (c) leakage currents and (d) fatigue curves.

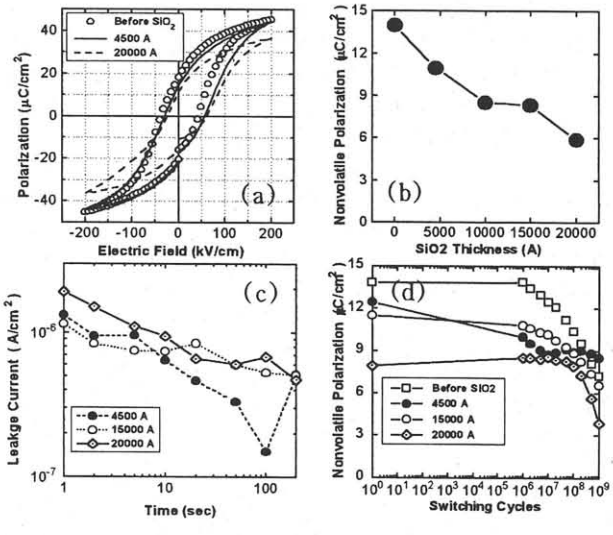


Figure 4. The ferroelectric properties of Pt/PZT/Pt capacitor according to ECR CVD SiO_2 deposition thickness; (a) hysteresis loops, (b) nonvolatile polarization, (c) leakage currents and (d) fatigue curves.

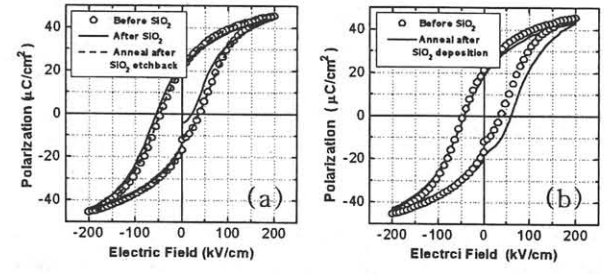


Figure 5. The O_2 anneal effect of Pt/PZT/Pt capacitor degraded by ECR CVD SiO_2 deposition ; (a) 450℃ 30min anneal under O_2 ambient after the etchback of SiO_2, (b) 450℃ 30min anneal under O_2 ambient before the etchback of SiO_2.