

## Effect of Cap-Metals on Co Salicide Process

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### Abstract

A Co salicide process using TiN-cap metal reduces the sheet resistance in narrow gate, source and drain regions. However, the detailed mechanism of the cap metal has not been well explained. We investigated various Co salicide processes and clarified the effect of the cap-metal. We found that the Co salicide process without cap-metal was very sensitive to the oxygen, even in very small concentration in the annealing chamber. We found that the cap-metal did not work as a promoter of the silicide reaction through metal stress, but did work mainly as a barrier to oxidation. Using these findings we demonstrated a low sheet resistance in narrow regions down to 0.075  $\mu\text{m}$  with several methods.

### 1. Introduction

In deep-submicron CMOS devices the reduction of parasitic resistances using a self-aligned silicide (salicide) process is a key issue for high speed operation <sup>1)</sup>. Recently, it has been reported that a Co salicide process with TiN-cap metal can successfully reduced the gate sheet resistance down to a gate-length of 0.075  $\mu\text{m}$ . The mechanism of the TiN-cap, however, was not fully understood and rationalized as the effects from oxidation prevention and the stress of the cap-metal <sup>2, 3)</sup>. Given that we would like to mass produce these devices, it is important to clarify the mechanism.

In this paper, we first discuss the degradation mechanism of the conventional Co silicide process. That is, why we could not reduce the sheet resistance. We examine the effects of oxidation by varying the amount of oxygen in the annealing chamber <sup>4)</sup>. We also observe the surface condition of poly-Si before metal sputtering, which might be damaged by many wafer processes <sup>5)</sup>. Then we examine the cap-metal effects using various cap-metal stresses. Using these experiments, we demonstrate several Co salicide processes which allow for a low sheet resistance.

### 2. Experiment

We performed various processes which could possibly enhance or retard the silicide reaction to determine the formation mechanism. To investigate the influence of the poly-Si gate surface conditions on the Co silicide reaction, we fabricated two types of gates; a conventional poly-Si gate and a SiN-blocked poly-Si gate (Fig. 1). After side-wall etching using  $\text{CF}_4$  and  $\text{CHF}_3$  gases, the SiN-block was removed by wet etching. The

SiN-blocked process could prevent process damage, especially induced by over etching of the side-walls. After HF treatment 10-nm-thick Co was sputtered to form 35-nm-thick  $\text{CoSi}_2$ . To investigate the influence of cap-metal stress on the reaction, we used a 30 nm TiN,  $\text{W}_2\text{N}$ , or W film with various stress intensities as a capping metal on the Co film. Then to investigate the oxidation effect, annealing was performed in the several conditions. These environments included: in-situ vacuum annealing in a sputtering chamber at 550  $^\circ\text{C}$  for 5 min (base pressure:  $1 \times 10^{-5}$  Pa) and rapid thermal annealing (RTA) in Ar ambient at 550  $^\circ\text{C}$  for 30 sec (base pressure: 1.0 Pa) after breaking the vacuum to transfer the wafer from sputter chamber to RTA. After selective wet etching, we carried out a second RTA at 850  $^\circ\text{C}$  for 30 sec. We measured the gate sheet resistance with a 4-point probe and investigated the atomic profiles using secondary ion mass spectroscopy (SIMS), and analyzed the Si surface using scanning electron microscopy (SEM).

### 3. Results and discussions

#### 3.1. Influence of oxygen during annealing

Figure 2 shows the gate sheet resistance after the Co salicide process without cap-metal. To investigate the influence of oxygen in the annealing chamber, We performed the first annealing in the various atmosphere, such as UHV with in-situ vacuum, Ar ambient, and Ar with a 1%  $\text{O}_2$  ambient. The Ar (1%  $\text{O}_2$ ) annealing process showed the highest sheet resistance for all gate lengths. This was because the Co film is easily oxidized with only a small amount of oxygen in the annealing chamber. The annealing in an Ar ambient could reduce

the sheet resistance in the large-gate regions but increased it at a gate length of less than 0.3  $\mu\text{m}$  long. The SEM photograph of this surface shows that at the 0.2- $\mu\text{m}$ -long gate, the edge of the silicided surface was rougher than the center, and moreover, at 0.1  $\mu\text{m}$  the whole surface became rough (Fig.3). It seems that silicide reaction speed is degraded at the edge of the poly-Si gate and Co becomes susceptible to oxidation in the RTA apparatus whose base pressure is not so low. By in-situ UHV annealing the sheet resistance was perfectly reduced down to a gate-length of 0.075  $\mu\text{m}$ . This result is consistent with recent reports on high-temperature sputtering followed by in-situ annealing process <sup>4</sup>). Therefore, without the cap-metal process, an oxygen-free condition is very important for the first annealing step.

### 3.2. Influence of surface condition

Next we examined the effect of the poly-Si gate surface condition on the Co silicide process. Usually, the surface of the poly-Si gate was contaminated and damaged by the many wafer processes, especially by side-wall over etching (Fig.1(a)). After the side-wall etching process, heavy F and C contamination was observed. It is also difficult to completely remove contamination by a post cleaning process. To investigate the influence of this damaged surface, we fabricated a damage-free poly-Si surface using a SiN-block process (Fig.1(b)). This process could decrease the physical damage and the concentration of F atoms on the poly-Si surface (Fig.4). This process achieved a low sheet resistance after the Co silicide process, even with annealing in the Ar ambient in the RTA chamber (Fig.5). We consider that the silicide reaction speed with a clean Si surface is higher than that of a damaged surface, therefore, even with the Ar ambient annealing process the silicide reaction could be finished before the oxidation of the Co film surface proceeds.

### 3.3. Effect of cap-metal

The TiN-capped process is an attractive way to reducing the sheet resistance. The effect of the TiN-cap can be explained as a barrier to oxidation and a silicide reaction promoter due to the strong stress. However, the effect of stress was not clear, and we did not know what kind of metal provides as the best cap film. We studied the effects of cap-metal stress on the silicide reaction. Cap-metals with various magnitudes and types of stress were prepared as shown in Figure 6. However, the resultant sheet resistances were almost the same, and low enough despite the all cap-metals (Fig.7). From this, we determined that the cap-metal works only as a barrier to oxidation species and has no effect on metal stress. Therefore, the cap-metal is not limited to a TiN film. This means that we can use any metal which does not react with Co to prevent the oxidation.

## 4. Conclusion

The Co silicide process is strongly influenced by the oxygen during the formation annealing and the Si surface condition. Using a SiN-blocked poly-Si process, we demonstrated a low gate sheet resistance. This is possible because the silicide reaction is fast enough that the oxidation has no influence. We succeeded in reducing the sheet resistance using W and W<sub>2</sub>N cap metals as well as TiN. This was because the silicide reaction was not related to the stress of the cap metals. The cap metal works as a barrier to the oxidation species.

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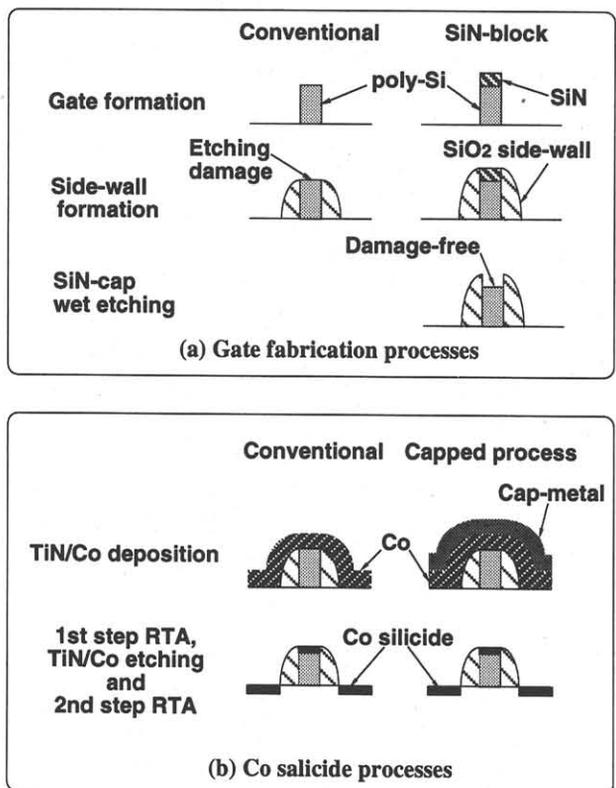


Fig. 1. Gate fabrication and Co silicide processes.

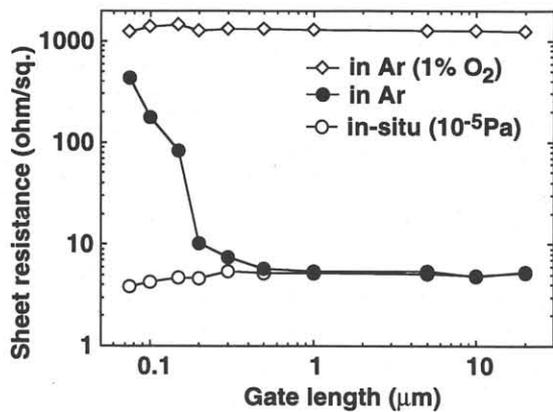


Fig. 2. Gate sheet resistance of Co silicide with varying annealing conditions.

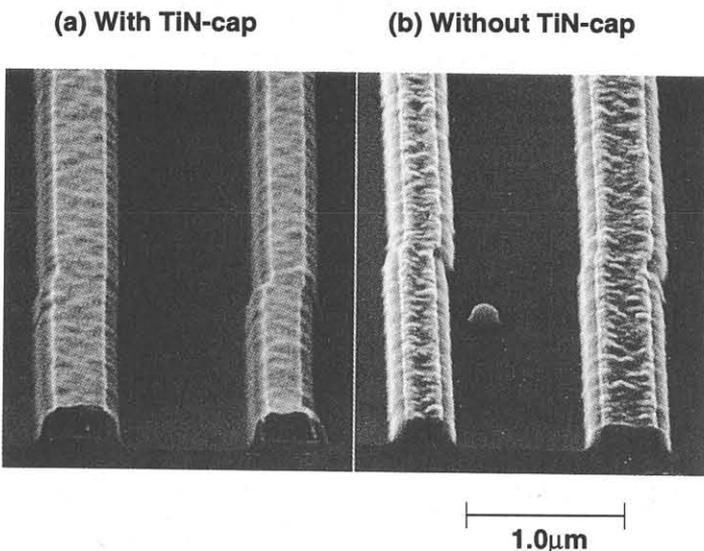


Fig. 3. SEM observations of Co silicide films (a) with and (b) without TiN-cap in Ar annealing.

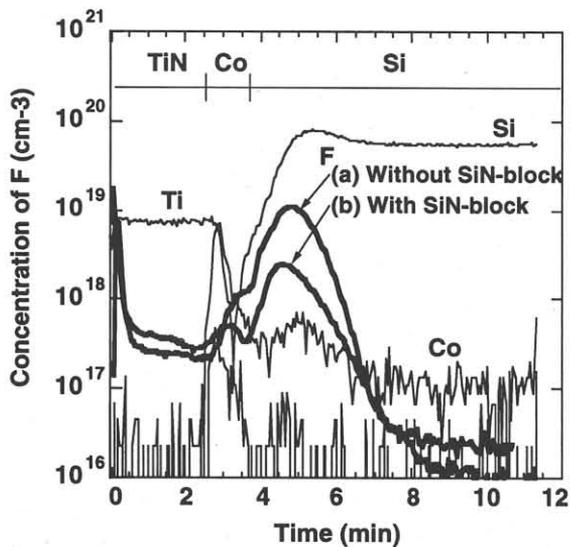


Fig. 4. Analysis of impurities by SIMS.

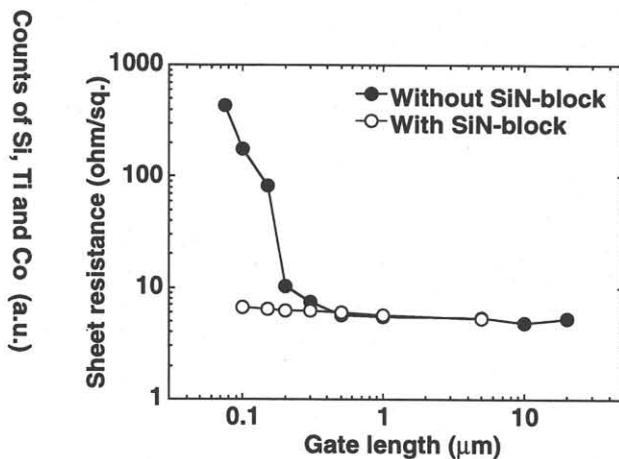


Fig. 5. Gate sheet resistance of Co silicide on poly-Si gate with/without SiN-block.

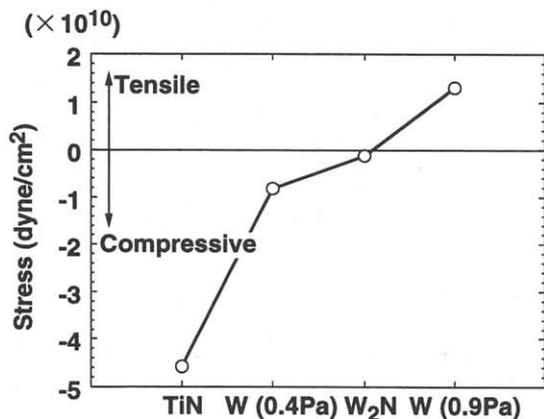


Fig. 6. Various film stress.

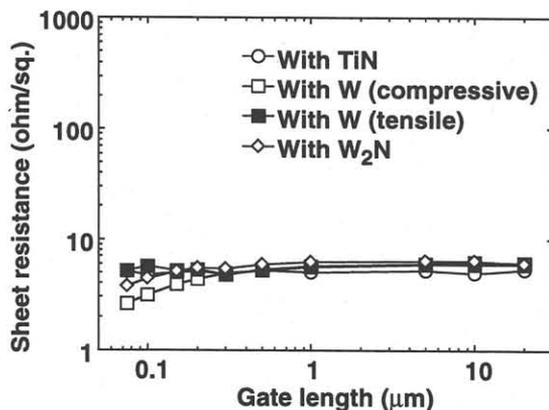


Fig. 7. Gate sheet resistance of Co silicide with several cap films on poly-Si gate without SiN-block.