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# Formation of Ultra-Shallow and Low-Leakage $p^+n$ Junctions by Low-Temperature Post-Implantation Annealing

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Ultra-shallow and low-leakage junctions have been successfully formed by $BF_2^+$ implantation at 25keV and following low temperature annealing (500°C). The junction depth is about 50nm and the leakage current is as low as $1.97 \times 10^{-9} A/cm^2$. This low temperature process becomes possible by suppressing the generation of the end-of-range damage by eliminating wafer surface contamination during ion implantation and reducing substrate dopant impurity. However, the influence of fluorine on the annealing behavior becomes problem.

## 1. INTRODUCTION

In order to form ultra-shallow junctions for future high-speed and scaled-down device structures, such as metal-substrate SOI metal-gate CMOS structure[1], reduction in the annealing temperature after ion implantation is essential. Usually, ion implanted junctions annealed at temperatures below 800°C are known to exhibit large leakage current[2] due to great amount of remaining end-of-range damage[3]. However, in arsenic implanted $n^+p$ junctions, it has been reported that the leakage current of the junctions after annealing at a temperature as low as 450°C can be reduced to the level for practical use by employing ultra clean ion implantation technology in which the wafer surface contamination during the ion implantation process has been extensively eliminated[4,5]. Furthermore, influence of boron in the substrate on the end-of-range damage has been clarified, and by reducing the substrate boron concentration to the level of $10^{14}$ atoms/cm$^3$, excellent $n^+p$ junction characteristics has been obtained[6].

Then the purpose of this paper is to present our success in forming ultra-shallow and low-leakage $p^+n$ junctions by $BF_2^+$ implantation followed by furnace annealing at 500°C applying the above technical advancement of arsenic implanted junctions. At first the annealing property of $BF_2^+$ implanted layers at low temperatures is demonstrated by the measurement of the sheet resistance, the carrier profile, and the crystallinety of the surface after annealing. It is also mentioned about the influence of fluorine in $BF_2^+$ implanted layers on the recrystallization behavior compared with layers implanted by $B^+$ after $Si^+$ pre-amorphization. Finally the leakage current of the $BF_2^+$ implanted junctions formed on high resistivity wafers is shown.

## 2. EXPERIMENT

An ultra clean ion implanter having a background pressure of $10^{-10}$ Torr and background metallic contamination level below $10^{10}$ atoms/cm$^2$ under typical source/drain implantation conditions was employed for the experiment[4,5].

For the investigation of annealing behavior of $BF_2^+$ implanted layer, n-type (100), 0.8-1.2 Ω·cm, Cz wafers were implanted with $BF_2^+$ at 25keV with a dose of $2 \times 10^{15} cm^{-2}$. In order to study the influence of fluorine, $B^+$ implantation was performed to the same wafers, which surfaces had been pre-amorphized by $Si^+$, at 25keV with a dose of $6.83 \times 10^{15} cm^{-2}$ resulting the same peak concentration of boron atoms as $BF_2^+$ implantation. The pre-amorphization was conducted in three-steps, namely $1 \times 10^{15} cm^{-2}$ at 25keV, $2.63 \times 10^{15} cm^{-2}$ at 75keV, and $4.1 \times 10^{15} cm^{-2}$ at 125keV in order to fully amorphize the layer from the depth needed to include the whole $B^+$ profile up to the surface. The annealing was performed in a furnace of nitrogen ambient at temperatures ranging from 450°C to 1000°C.

For the measurement of the leakage current of the above junctions, another samples were prepared on n-type (100), 10-20 Ω·cm, FZ wafers.

## 3. RESULTS AND DISCUSSION

**Figure 1** shows the dependence of the sheet resistance of $BF_2^+$ implanted layers on annealing time at 450, 480, 500 and 550°C. Initially, $BF_2^+$ implanted surface has an amorphous layer of 35nm thick and the implanted boron is not activated. However, by the solid phase epitaxy, reordering starts from amorphous crystalline interface and boron is also incorporated into the lattice site. The sheet resistance of 450, 480, 500 and 550°C annealed samples are saturated for 36h, 9h, 4h and 0.5h, respectively. These times are about one order of magnitude longer than those for arsenic implanted layer[7].

In **Fig. 2**, sheet resistance of $BF_2^+$ implanted layers after annealing is plotted as a function of annealing temperature. The annealing time was

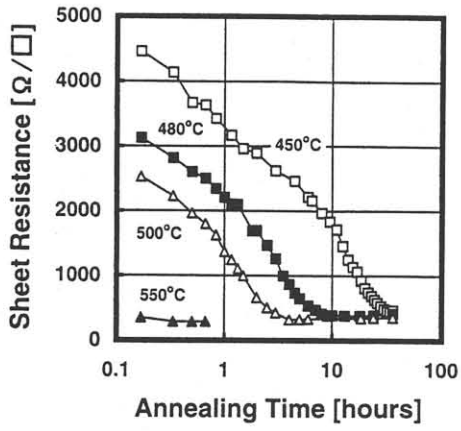


**Fig. 1** Sheet resistance of $BF_2^+$ implanted layers plotted as a function of the annealing time.

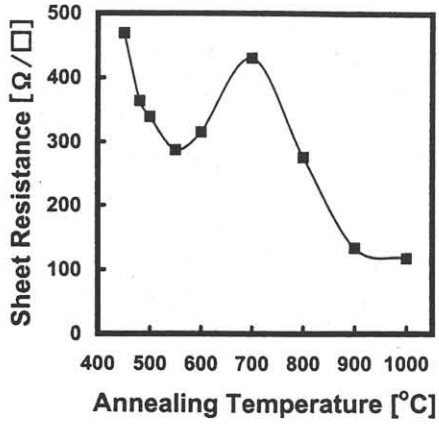


**Fig. 2** Sheet resistance of $BF_2^+$ implanted layers plotted as a function of annealing temperature.

36h at 450°C, 9h at 480°C, 4h at 500°C, 0.5h at 550°C, 1h at temperatures from 600 to 900°C and 30min at 1000°C. The sheet resistance decreases in annealing temperature from 450°C to 550°C. However, from 600°C, the resistance turns to increase and takes a peak at 700°C. Presumably, carrier deactivation occurs at 600-700°C[4]. The carrier concentration profiles of the junctions annealed at 450-800°C are shown in **Fig. 3**. It is clearly seen that the carrier concentration of 700°C annealed sample decreases in the range of 30-40nm from the surface, while that of 800°C annealed sample keeps higher carrier concentration. Furthermore, it can be also seen that the defect induced enhanced diffusion occurs at 700 and 800°C. In order to prevent the carrier deactivation and the enhanced diffusion, the annealing must be performed below 600°C.

At 450, 480 and 500°C, very shallow junctions about 50nm are formed without any enhanced diffusion (**Fig. 3**). However, while implanted boron is activated up to the surface at 480 and 500°C, boron in 450°C annealed sample is not completely activated at the surface region. **Figure 4** shows the photographs of RHEED patterns of these surfaces.

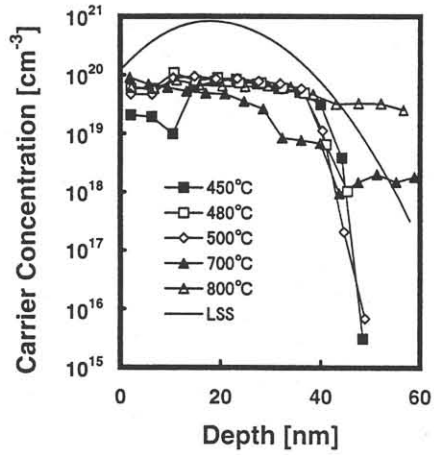


**Fig. 3** Carrier concentration profiles of $BF_2^+$ implanted layers after annealing.

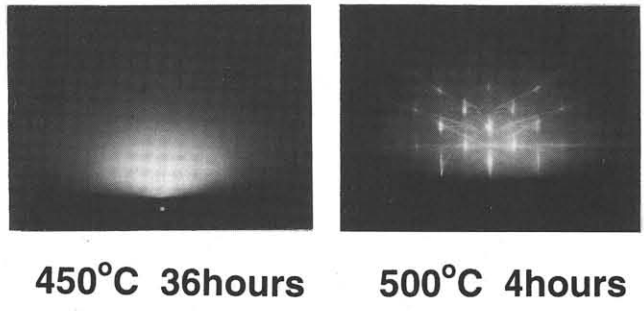


**Fig. 4** Photographs of RHEED (Reflection High Energy Electron Diffraction) pattern of $BF_2^+$ implanted surface after annealing at 450°C for 36 hours and 500°C for 4 hours.

At 500°C, excellent streaks and Kikuchi lines can be observed. But the pattern of 450°C indicates that the surface is still amorphous in accordance with the carrier profile shown in **Fig. 3**. Hence, the annealing time of 36h at 450°C is not enough to restore the crystallinety. Fluorine in the implanted region would severely influence on the annealing property.

In **Fig. 5**, the average regrowth rate of amorphous layer formed by $BF_2^+$ implantation is plotted as a function of the annealing temperature compared with that of $B^+$-implanted pre-amorphized layer which thickness is 260nm. The regrowth rate was calculated dividing the thickness of the initial amorphous layer by the annealing time necessary to saturate the sheet resistance. It is clearly seen that the regrowth rate of $BF_2^+$ implanted layer is about one order of magnitude smaller than that of $B^+$ implanted pre-amorphized layer. This result indicates that the presence of fluorine reduces the velocity of epitaxial regrowth. In **Fig. 6**, the peak carrier concentration of the junctions formed by both ion species is plotted as a function of annealing temperature. The peak carrier concentration of the $BF_2^+$ implanted layer is about 50% smaller than

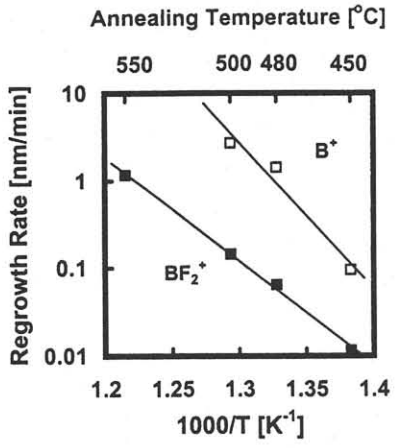


**Fig. 5** Annealing temperature dependence of average regrowth rate of amorphous layer formed by $BF_2^+$ implantation and that of $B^+$-implanted pre-amorphized layer.

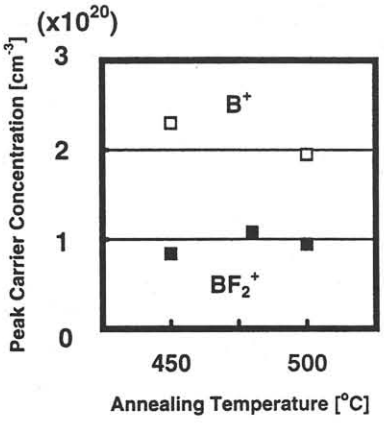


**Fig. 6** Peak carrier concentration of $BF_2^+$ implanted layers and $B^+$ implanted $Si^+$ pre-amorphized layer after low temperature annealing.

that of $B^+$ implanted layer through the whole annealing temperature range. Therefore, fluorine also degrades the activation yield of the implanted boron.

In **Fig.7**, the reverse-bias current densities at 5V of $p^+n$ junctions formed by each ion species are plotted as a function of annealing temperature. In this experiment, high resistivity n-type substrate was used to suppress the substrate dopant induced damage[6]. The leakage current of junctions formed by $BF_2^+$ implantation keeps below $10^{-9}$ A/cm$^2$ at the whole temperature range. At 500°C, the leakage current level is as low as $1.97\times10^{-9}$ A/cm$^2$. This level is about three orders of magnitude smaller than previously reported data[2]. On the other hand, the leakage current of $B^+$ with $Si^+$ pre-amorphization drastically increases below 700°C. It is speculated that the annealing-out of the end-of-range damage caused by high energy $Si^+$ ion during pre-amorphization would be very difficult and the damage would remain in the space charge region of the junction after low-temperature annealing. So, it is clear from the present results that elimination of fluorine in the implanted region is necessary,

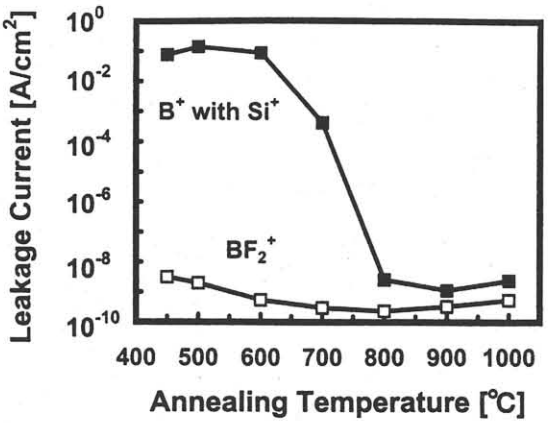


**Fig. 7** The leakage current at 5V of $p^+n$ junctions formed by $BF_2^+$ implantation and $B^+$ implantation with $Si^+$ pre-amorphization plotted as a function of annealing temperature.

however, the combination of pre-amorphization and $B^+$ implantation is not acceptable because the damage induced by the $Si^+$ implantation becomes much more critical. The development of alternative method to eliminate fluorine in $BF_2^+$ implantation is desired to realize total low temperature processing.

## 4. CONCLUSION

The annealing behavior of $BF_2^+$ implanted layer at low temperatures is demonstrated. From the point of view on shallow junction formation, the annealing temperature below 600°C is required in order to prevent the defect induced enhanced diffusion and the carrier deactivation. It is also pointed out that fluorine accompanying with boron have a bad influence on the annealing behavior, such as regrowth velocity and peak carrier concentration. By 500°C annealing, we can form ultra-shallow and low leakage junctions which junction depth is about 50nm and the leakage current is as low as $1.97\times10^{-9}$ A/cm$^2$.


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