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A Novel LOCOS-Trench Combination Isolation Method for Maximum Chemical Mechanical Polishing(CMP) Process Window

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A novel isolation technology which combines LOCOS in the wide field region and trenches in the narrow region, and finishes the process with Chemical Mechanical Polishing(CMP) has been developed. It requires two photo steps for isolation: The first one is the same as the conventional active area defining photo step and the second one is the peripheral area opening which does not need the precise control of either the size or the misalignment. By optimizing the LOCOS oxide thickness before trench etching, a condition for minimum dishing at the CMP step can be obtained.

1. INTRODUCTION

In order to make the planarized field area in the device isolation structure, LOCOS-Trench combined processes have been suggested[1,2] and the necessity of the CMP step to eliminate the kinks was also presented[3]. However, the non-memory devices which have very randomly allocated active and field regions require the well to well trench isolation, which needs a deeper trench. Therefore, the conventional processes such as trench etching in all over the places, the active area opening and the dry etch-back pre-planarization before CMP is coming to be more difficult since the bigger step height and consequently the thicker CVD oxide filling is required and it could cause untolerable dishing effect[4]. Therefore, a process technology which has LOCOS oxide in the wide field region and the trenches at the center of the LOCOS oxide in the narrow field region has been proposed[5]. By the same year, maintaining good gate oxide characteristics without having LOCOS oxide at both edges of the trenches were anticipated[6] and confirmed[7] at the next year using short oxidation before trench etching and the trench top corner rounding.

In this report, we propose a simpler LOCOS/Trench combined isolation method which has simple trenches in the narrow field region and the LOCOS oxide in the wide field area to maximize the CMP process window.

2. EXPERIMENTAL

At first, pad oxide and SiN layer were deposited and etched in the field area for active area definition. Thin SiN layer(30 nm) was again deposited(fig.1 (a)), and the wide field area was opened and SiN layer was etched(fig.1 (b)). Then, the oxidation of the field area in H_2O ambient was carried out with the thickness of 350 nm(fig.1 (c)). Thin SiN layer was anisotropically etched to open the field area in the narrow field region and trench etching was performed(fig.1 (d)). Slight oxidation of the trench sidewalls was done to eliminate the defects which might be generated during the trench etching step, filling of the trenchs with the CVD oxide, and the CMP were carried out(fig.1 (e). Finally, SiN and pad oxide were removed.

3. RESULTS AND DISCUSSION

Figure 2 shows the SEM profiles in each process step as explained in fig.1. As shown in fig.2 (a), thin SiN layer works well as a mask layer against the oxidation in the narrow field region during the LOCOS oxidation step, and fig.3 which shows the grown field oxide thickness according to the overlying SiN thickness confirms the process security. In the LOCOS step, by choosing an optimum field oxide thickness with considering the step height in various active and field arrays, the dishing effect can be minimized as schematically shown in fig.4. At the thin SiN etch step(between fig.2 (a) and (b)), LOCOS oxide is also etched because the selectivity of SiN layer to SiO2 layer is known to be not very good. However, the End Point Detection(EPD) at the substrate Si is well performed due to the high selectivity to Si layer.

The higher CMP rate of the SiO_2 layer to SiN layer is known to be a major reason for the dishing, but using this technology, the oxide surface level can be raised in the wide field region to minimize the dishing problem. In addition, thermal oxide in the wide field region has the lower polishing rate than that of the CVD oxide. These factors widen the process window at the CMP step. These are well proved in fig.5 which shows more uniform field oxide thickness distribution after the CMP than that of the conventional trench isolation with dry etch-back preplanarization, although the new process requires more CMP for the final planarization.(It is generally known that the uniformity is getting worse as the amount of the CMP.)

Electrical properties of the trench isolated devices are thought to be the same as the ones with the conventional trench isolation. Threshold voltage characteristics(fig.6) with respect to the gate widths in the trench isolated transistors show that the Inverse Narrow Width Effect(INWE) disappeared in the transistors with rounded trench top corners(fig.7)

4. CONCLUSION

A new LOCOS-Trench combined isolation technology which has the wider process window for CMP than the conventional trench isolation has been developed and its characteristics were observed. By keeping with most of the conventional processes, and adding a quite simple photo, a thin SiN layer deposition, and an etching step, dishing

problem that has been one of the biggest obstacle for isolation CMP process was improved. It is expected that this process is useful in the devices such as logic chips which require the deep trenches and wide field regions.

5. REFERENCES

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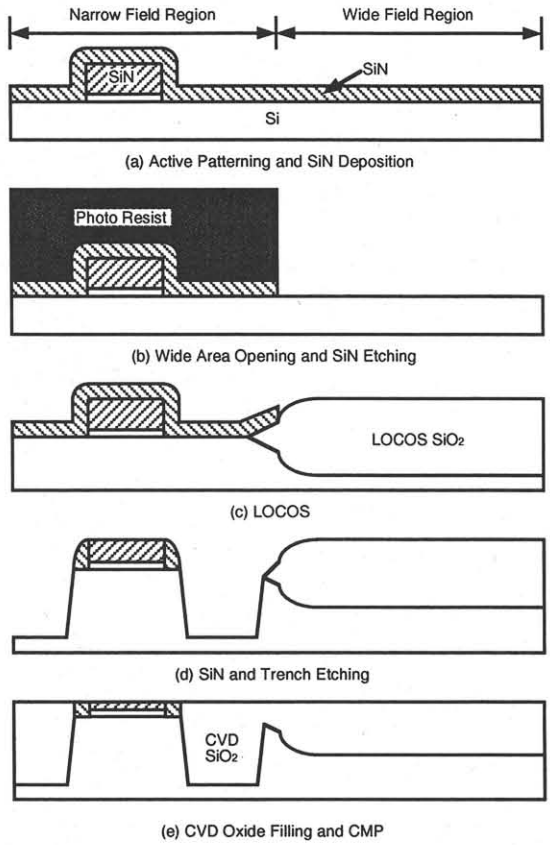


Figure 1. Process steps.

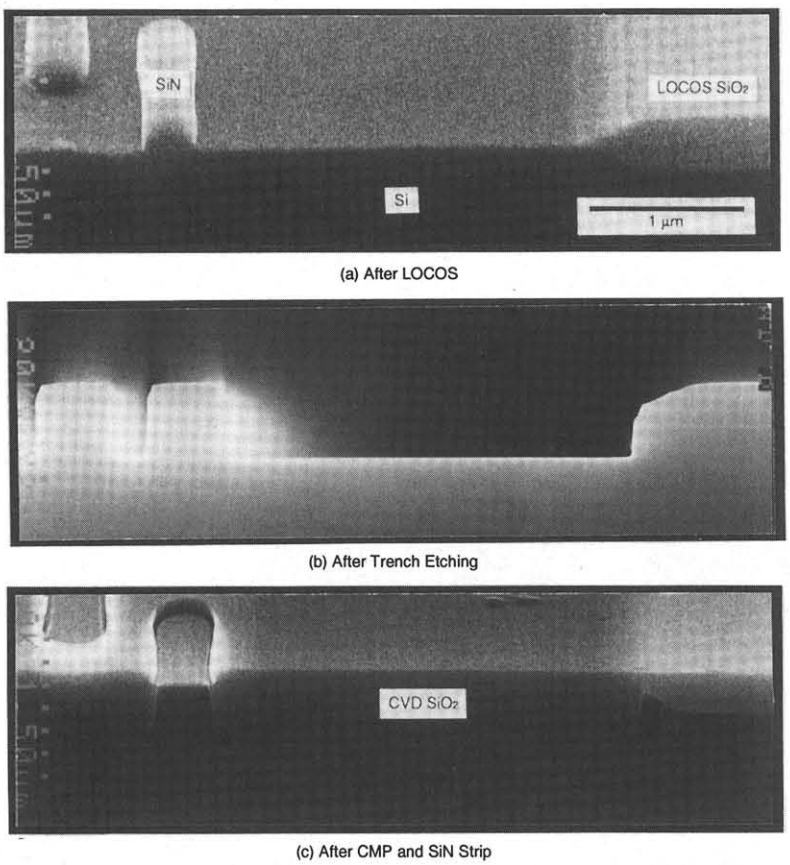


Figure 2. SEM cross-sectional micrographs in critical steps.

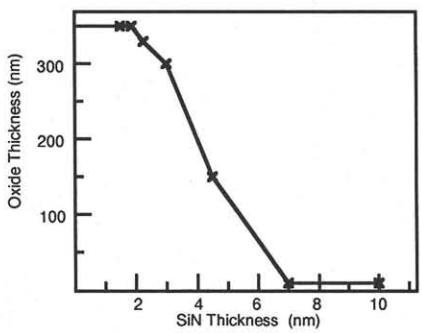


Figure 3. Oxide thicknesses grown on top of the SiN layers. Pad oxide was 6 nm and 350 nm thick oxide was grown on a bare Si wafer.

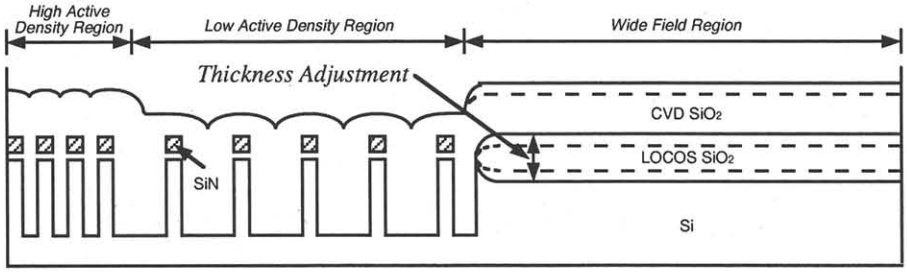


Figure 4. Schematic illustration of the relative step heights where there are two kinds of cell arrays. Optimum field height can be obtained by adjusting the LOCOS thickness.

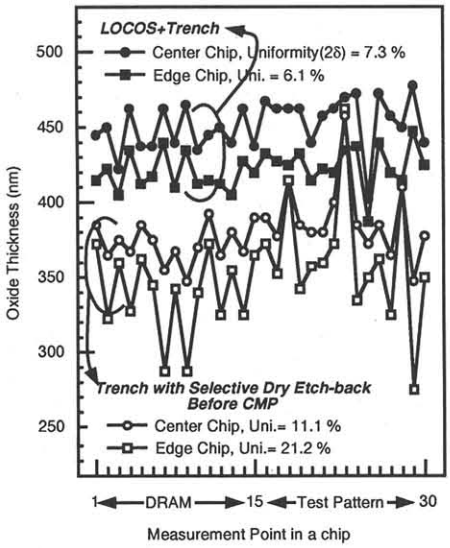


Figure 5. Field oxide thicknesses after the CMP in a unit test chip. Points are uniformly located in a measured area. Chip width is 1.46 cm and length is 1.82 cm.

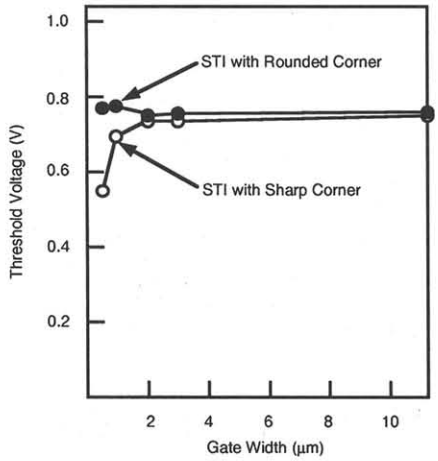
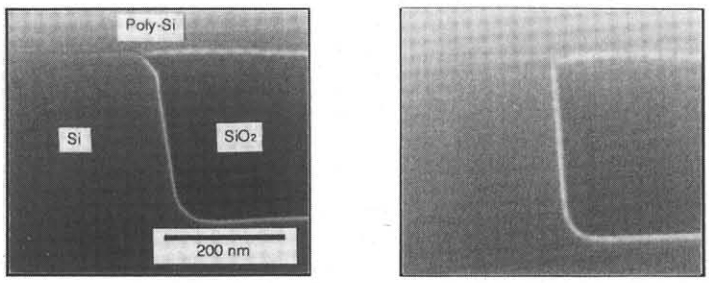


Figure 6. Threshold voltage characteristics of NMOSFETs with respect to the gate width. V_b = 0 V, V_d = 0.1 V, and gate length = 10 μm.



(a) Rounded Top Corner Case (b) Sharp Top Corner Case

Figure 7. SEM cross-sectional micrographs of trench edges.