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Electrical Characteristics of Ultra-Fine Trench Isolation Fabricated by a New Two-Step Filling Process

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Abstract Ultra-fine trench isolation with excellent electrical properties was formed by using a new fabrication process. A void-free shape and less thinning of the field oxide were realized by two-step filling with TEOS at a lower portion and high density CVD-SiO2 as a upper capping layer. The breakdown voltages were as high as 8 V for the field space as narrow as 0.13 μm. The subthreshold characteristics of the MOSFET were kink-free. The threshold voltages of parasitic MOSFETs, furthermore, were more than 6 V even with no channel stop implant.

1. Introduction

In semiconductor technology below the subquarter-micron scale, trench isolation will prove its real worth due to having no significant lateral extension of field oxide and independent controllability of its depth and width, as compared to LOCOS isolation [1].

Filling a trench with oxide, however, is an important but unestablished step in the fabrication process of the trench isolation which has a very narrow space and a high aspect ratio, because the shape of the field oxide significantly affects the electrical characteristics of both the isolation and the MOSFETs. Voids in the field oxide may cause the shorts between MOSFETs when gate polysilicon remains in the void. On the other hand, thinning of the field oxide at the channel edges, which is enhanced by the voids for ultra-fine isolation, results in anomalous MOSFET characteristics [2,3].

To solve these problems, we have developed a novel trench isolation process with a high density oxide capping layer (HIDOC).

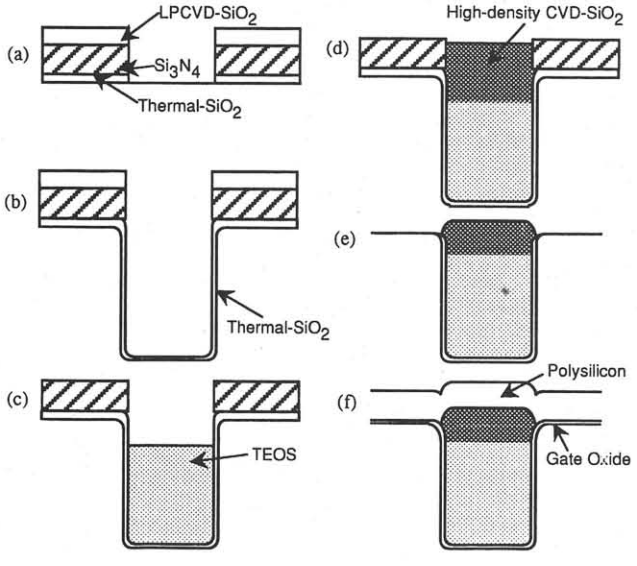

Fig. 1 HIDOC Process.

2. Fabrication Process with HIDOC

The process sequence is schematically illustrated in Fig. 1. A hard mask composed of LPCVD-SiO2/Si3N4/thermal-SiO2 was patterned down to 0.13 μm by using EB lithography and a dry etching technique (a). A trench of about 0.3 μm deep was etched by a conventional RIE technique, followed by sidewall oxidation (b). The aspect ratio is more than 2 for the minimum field space of 0.13 μm.

The next step, filling the trench with oxide, is important to obtain a trench having the very narrow width and the high aspect ratio required. In a usual filling process using TEOS, seams are formed at the central portions in the field spaces, which are easily etched by diluted HF solutions which are used to remove the thermal-SiO2 mask. As a result, void formation occurs [3].

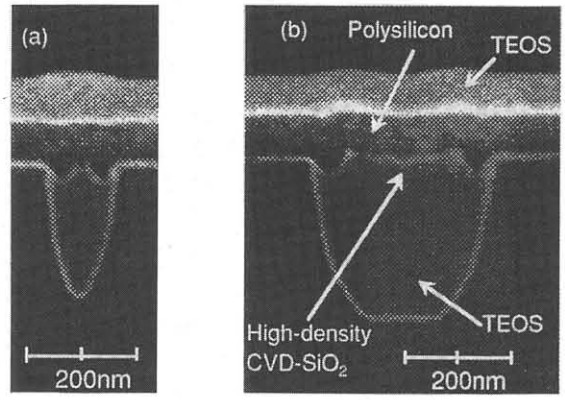

Fig. 2 SEM cross-sectional views of trench isolation of field spaces of (a) 0.13μm and (b) 0.35μm.

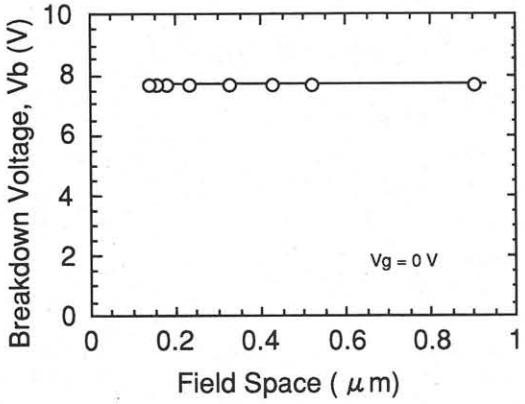

Fig. 3 Dependence of breakdown voltage on field space.

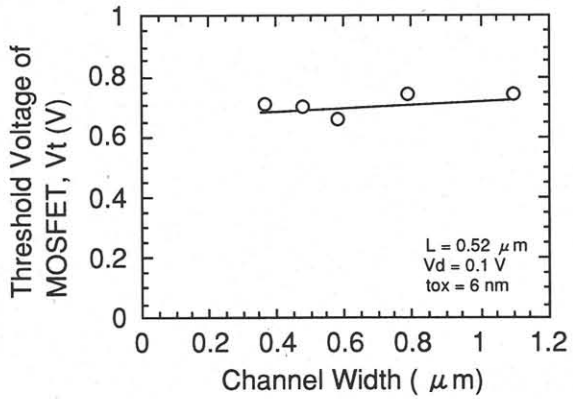

Fig. 5 Dependence of MOSFET's threshold voltage on channel width.

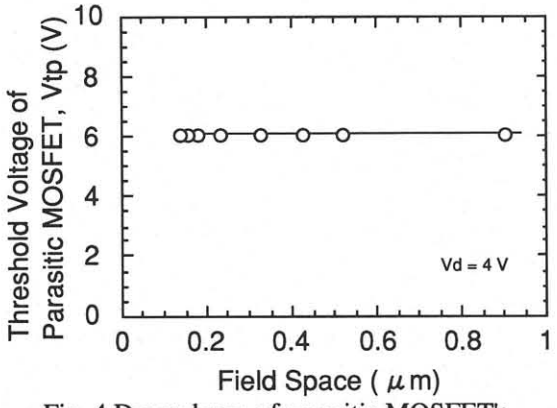

Fig. 4 Dependence of parasitic MOSFET's threshold voltage on field space.

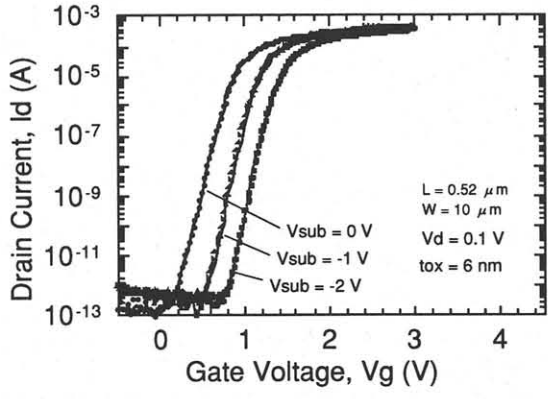

Fig. 6 Subthreshold characteristics of MOSFET.

Therefore, we developed a two-step filling process by taking advantage of two types of oxide, TEOS giving conformal step coverage properties, and CVD-SiO2 giving high density. The step in this process begins with filling with LPCVD-TEOS. The oxide was etched back below the silicon surface to decrease the aspect ratio of the trench (c). Next, hard, high density CVD-SiO2 was deposited as a capping layer and planarized by the etch-back (d). Finally, the mask was removed by wet etching without making any voids (e). Special sidewall doping to suppress parasitic MOSFETs at the channel edges was not used.

After formation of the isolation space, the NMOSFET process begins with the well, channel stop, and channel implants of boron ions. For some wafers, the channel stop implant was eliminated. Polysilicon was deposited and etched to form the transistor gate after formation of a 6-nm-thick gate oxide (f).

Figure 2 shows SEM cross-sectional views of the structures of field spaces of 0.13 and 0.35 μm. No remarkable voids are observed in the central portion. Moreover, edge shapes of the isolation do not depend on field space, because of no void formation.

3. Electrical Characteristics

The breakdown voltage (Vb) of as high as 8 V was maintained down to the ultra-narrow field spaces of 0.13 μm, as shown in Fig. 3. The parasitic MOSFET's threshold voltage (Vtp) was more than 6 V, as shown in Fig. 4.

Next, we show the characteristics of the NMOSFETs. As shown in Fig. 5, the threshold voltage (Vt) at a drain voltage (Vd) of 0.1 V is hardly changed for channel widths between 0.35 and 1.1 μm. Moreover, Fig. 6 shows the kink-free subthreshold characteristics of the NMOSFET with a 0.5-μm-long, 10-μm-wide channel for various substrate voltages (Vsub). This result shows that the present corner edge shapes do not degrade electrical properties of the NMOSFETs. Simulation indicates that the electron concentration at the channel edge is almost the same as that at the channel center, as shown in Fig.7. Thus, we confirmed that field crowding at the channel edge, which induces anomalous subthreshold characteristics, is successfully suppressed. Figure 8, furthermore, shows the peripheral and area components (Jp and Ja) of the n+/p-well junction leakage current.

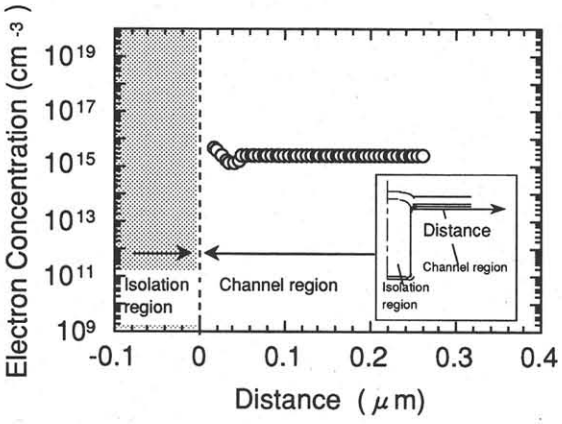

Fig. 7 Simulated electron concentration profile in the vicinity of the Si substrate surface.

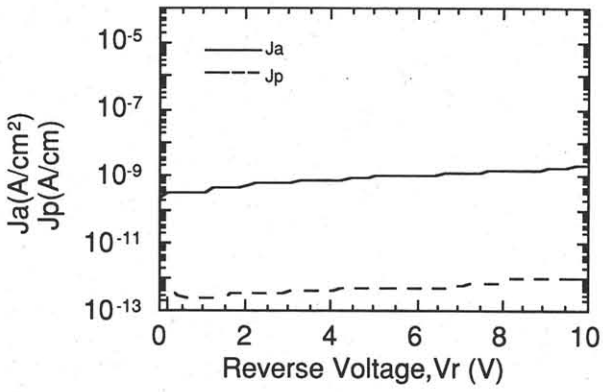

Fig. 9 Peripheral and area components (*Jp* and *Ja*) of junction leakage current without channel stop implant.

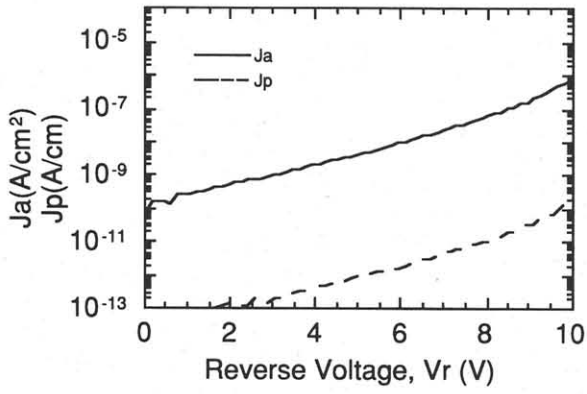

Fig. 8 Peripheral and area components (*Jp* and *Ja*) of junction leakage current .

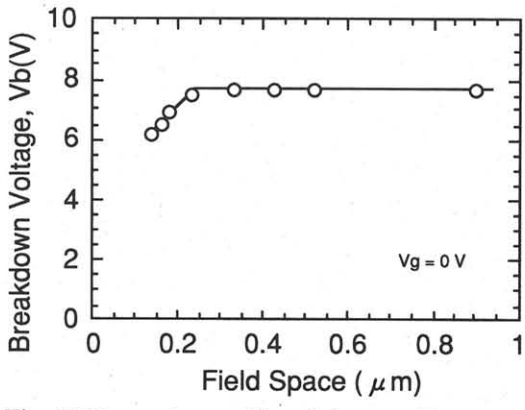

Fig. 10 Dependence of breakdown voltage on field space without channel stop implant.

We also examined the characteristics of the samples without the channel stop implant. Figure 9 indicates the leakage characteristics are drastically improved by eliminating the channel stop implant, though the Vb was somewhat degraded, as shown in Fig. 10. The good Vtp and kink-free subthreshold characteristics of MOSFET did not depend on the channel stop implant.

4.Conclusion

A new trench isolation technology using HIDOC has been developed. This process provides the excellent overall electrical properties, such as a high isolation breakdown voltage, a high parasitic MOSFET threshold voltage, and a kink-free MOSFET subthreshold characteristics. Without channel stop implant, moreover, the leakage characteristics are improved with little degradation in the breakdown characteristics. These excellent results indicate that this type of trench isolation is promising for ultra-large integration devices such as giga-bit scale DRAMs.

Acknowledgments

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