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A Novel Shallow Trench Isolation Technique

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Abstract

The shallow-trench isolation technology using a masking nitride layer, polysilicon refill, CMP process with high etch selectivity, and local oxidation of polysilicon is well-operated and absolutely bird's beak free. Although the CMP process results in dishing effect in wide field regions, the local oxidation of polysilicon can reduce the amount of dishing. The polysilicon-filled shallow-trench isolation process can also achieve an excellent uniformity across 6-inch diameter silicon wafers resulting from high etching selectivity of polysilicon to CVD oxide and SiN and low n^+/p junction leakage current. This simple and well-operated process provides a very promising candidate for shallow trench isolation.

Introduction

To realize the scaled, high-density, and high-performance VLSI devices and circuits, the isolation process becomes a key processing technique. The local oxidation of silicon (LOCOS) isolation has been widely utilized in the high density Dynamic Ramdom Access Memory (DRAM) device. However, the conventional LOCOS isolation process results in a large encroachment of field oxide (bird's beak) into the devices' active regions [1]. Therefore, the reduction of bird's beak encroachment in the active region of memory cell is the most important issue.

The oxide-filled trench isolation technology has been proposed to reduce the bird's beak [2,3]. However, the conventional resist planarization and RIE etch back process has cumulative tolerences associated with large film thickness [4]. The etch back of oxide-filled shallow trenches based on a chemical-mechanical polish (CMP) process has been proposed to circumvent this problem [4,5]. However, the CMP process shows problems with nonuniform polish and difficult control because there is no stopper for oxide etch-back [6]. Also, the CMP process results in dishing effect in wide field regions [5].

In order to overcome these problems mentioned above, a satisfying isolation technology for bird's beak free and well-controlled isolation process is required. This paper presents an absolutely bird's beak free and well-operated shallow trench isolation technique. It utilizes a masking silicon nitride layer, polysilicon refill, CMP process with high etching selectivity, and local oxidation of polysilicon to circumvent these problems.

Experimental

The polishing slurries (RODEL 2371 and SC-1) used in this experiment are colloidal silica in an aqueous KOH solution. Details on slurries' properties are listed in Table 1. Test structures of the shallow trenches were fabricated on p-type (100) silicon wafers.

Fig. 1 shows the schematic process sequence of polysilicon-filled shallow trenches. First, the trench mask was defined and then silicon trench (650 nm) was etched by a $Cl_2/O_2/SF_6$ plasma. After the removal of photo resist, wafers were cleaned. A 30 nm thick silicon dioxide was grown by dry oxidation at 925°C. This was followed by LPCVD SiN deposition of 30 nm. Subsequently, a 22 nm thick LPCVD oxide was deposited to passivate the SiN layer. Then, a 900 nm thick LPCVD polysilicon was deposited to refill the shallow trenches. After the shallow trenches were refilled, the polysilicon layer was polished at 4 psi (27.2 kPa) with a dilute 3:1 slurry B as shown in Fig. 2(b). After the CMP process, the wafers were cleaned. A 400 nm thick silicon dioxide was thermally grown by wet oxidation at 980°C as shown in Fig. 1(c). Then, the SiN layer was etched by a RIE process and the pad oxide was stripped by a buffer HF solution as shown in Fig. 1(d).

After the planarizatrion processes, wafers were cleaned. A 10 nm thick silicon dioxide was grown by dry oxidation at 900°C. Next, the screen oxide was stripped by a buffer HF solution. Then, arsenic implantation was performed through a 5 nm thick pad oxide at 60 Kev with a dose of $5x10^{15}$ cm^{-2}. After the implatation process, wafers were cleaned and a 550 nm LPCVD oxide was deposited at 700°C. Next, wafers were annealed in an O_2 ambient at 900°C for 15 min to form the n^+/p junction. After the contact holes and aluminum contact were performed, wafers were sintered in a N_2 ambient at 350°C for 30 min.

Results and Discussion

The etch selectivity of CVD oxide with respect to SiN is low (< 3) as shown in Fig. 2(a). Therefore, there is no stopper for oxide etch-back. The etch selectivity of polysilicon with respect to CVD oxide and SiN is shown in Fig. 2(a) and Fig. 2(b). Comparing with Fig. 2(a) and Fig. 2(b), the slurry B with higher KOH concentration and larger silica particles results in higher selectivity. The reason is that the large silica particles reduce the mechanical effect and the high KOH concentration enhances the chemical reactions. The etch selectivity of polysilicon to CVD oxide and SiN reaches 92 at 4 psi (27.2 kPa) with a dilute 3:1 slurry B. As a result, the CVD-oxide or SiN layer can serve as a stopper for polysilicon etch-back.

Fig. 3(a) shows the SEM micrograph of polysilicon-filled shallow trenches considered in this work after a CMP process at 4 psi (27.2 kPa) with a dilute 3:1 slurry B. The trench sidewalls and active regions are capped by a SiN layer. This CMP process is well-controlled due to high etching selectivity of polysilicon to CVD oxide and SiN. Fig. 3(b) shows the SEM micrograph of polysilicon-filled shallow trenches after the local oxidation of polysilicon and the pad oxide/SiN layer stripped. Absoloutely, there is no encroachment of field oxide into the devices' active regions because of the SiN layer serving as a mask to prevent the active regions and trench sidewalls from oxidation.

The dishing result of oxide-filled shallow trenches after a CMP process and the pad oxide / SiN layer stripped is shown in Fig. 4. Obviously, the CMP process results in dishing effect in wide field regions. This implies that in wide field regions, the reduction in the pressure is less significant due to the elasticity of the

pad [5]. It results in a continued polishing of oxide after the CVD oxide and SiN interface is reached. The dishing results of polysilicon-filled shallow trenches before and after local oxidation of polysilicon are also shown in Fig. 4. Also, the CMP process results in dishing effect in wide field regions. However, the local oxidation of polysilicon can reduce the dishing effect. Although the dishing effect makes the planarization difficult, it poses no serious problem for polysilicon-filled trench isolation considered in this work due to local oxidation of polysilicon.

Fig. 5 shows the dishing distribution for 100-μm wide field region across 6-inch diameter silicon wafers. The measured points are shown in the inset of Fig. 6. Obviously, the global deviation of oxide-filled shallow trenches is larger than that of polysilicon-filled shallow trenches. The global deviation of dishing of polysilicon-filled shallow trenches is less than 10%. Therefore, the polysilicon-filled shallow-trench isolation process considered in this work can achieve an excellent uniformity due to high etching selectivity of polysilicon to CVD oxide and SiN.

Fig. 6 shows the leakage current distribution of the n^+/p junction diodes (area = 0.01 cm^2). The n^+/p junction leakage current at 3.3 V of polysilicon-filled shallow trenches is comparable to that of the conventional oxide-filled shallow trenches. This implies that low defect density results from the novel process considered in this work.

Conclusions

The oxide-filled shallow-trench isolation technology based on a CMP process is difficult to control and results in poor uniformity. It also results in dishing effect in wide field regions. However, an absolutely bird's beak free and well-operated polysilicon-filled shallow-trench isolation technology based on a CMP process has been demonstrated successfully. The isolation process considered in this work can achieve an excellent uniformity. The CMP process also results in dishing effect in wide field regions. However, the local oxidation of polysilicon can reduce the amount of dishing. There is no stopper for oxide etch-back. However, high etch selectivity of polysilicon to CVD oxide and SiN can be achieved by using a slurry with a high KOH concentration and large silica particles. Selectivity is pressure-dependent. The polysilicon-filled shallow-trench isolation process can also achieve an excellent uniformity and low n+/p junction leakage current.The polysilicon-filled shallow-trench isolation process considered in this work is a very promising candidate for shallow trench isolation.

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Table 1

	slurry A	slurry B
type(RODEL)	SC-1	2371
PH	10.0~10.3	11.0~11.5
particle size (nm)	30	70~90
Wt. % solids	30	28
Viscosity (cps)	< 150	< 25

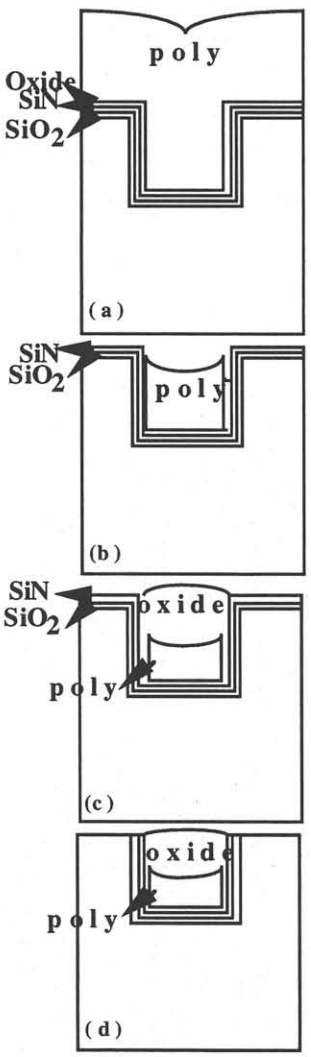
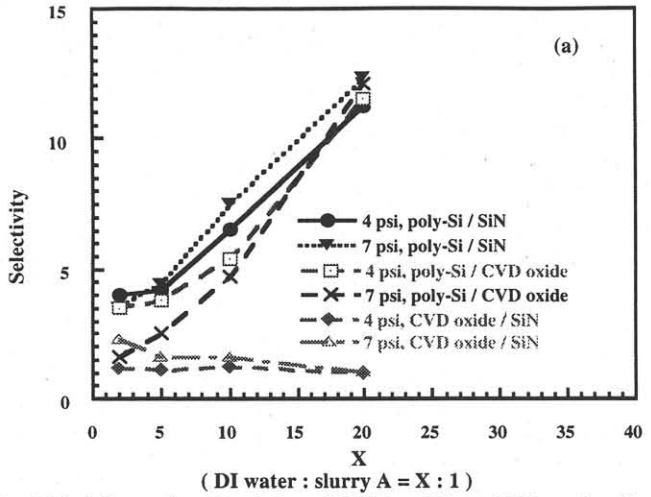
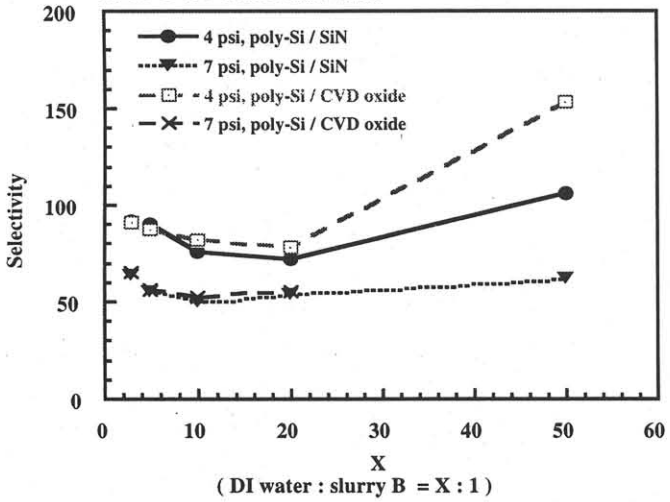


Fig. 1 The schematic process sequence of polysilicon-filled shallow trenches.



(DI water : slurry A = X : 1)

Fig. 2(a) The etch selectivity of CVD oxide to SiN, and poly-Si to CVD oxide and SiN.



(DI water : slurry B = X : 1)

Fig. 2(b) The etch selectivity of poly-Si to CVD oxide and SiN.

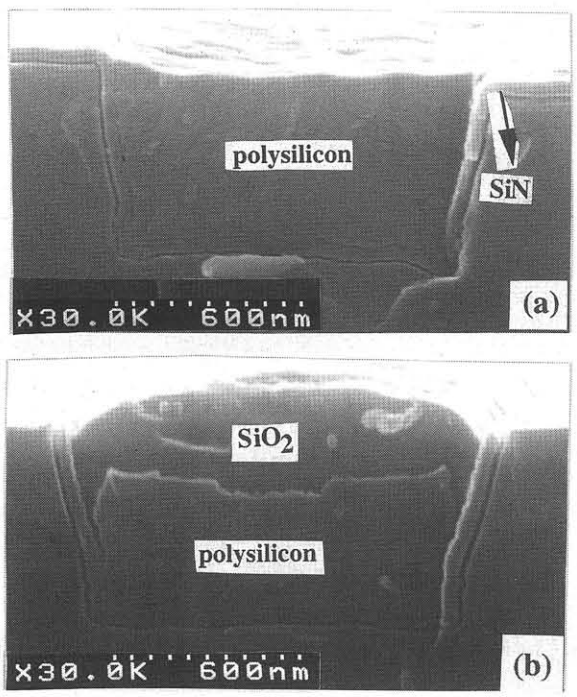


Fig. 3 The SEM micrographs (a) polysilicon-filled shallow trenches after a CMP process (b) polysilicon-fillled shallow trenches after a local oxidation of polysilicon and the pad oxide/SiN layer stripped.

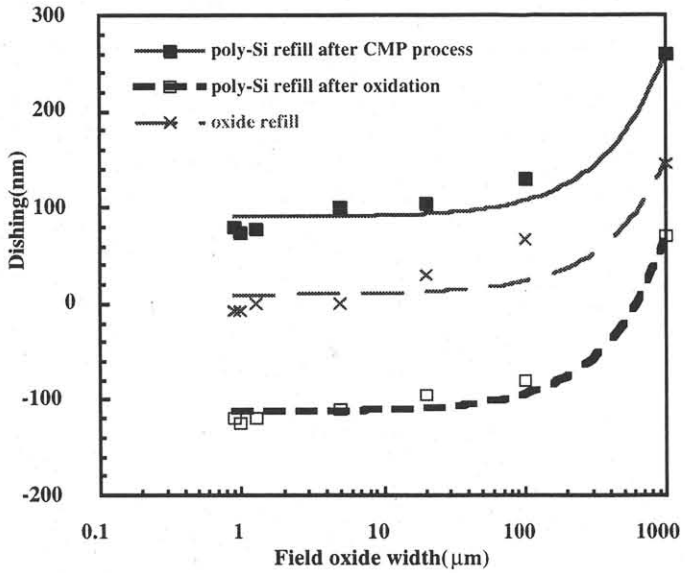


Fig. 4 The dishing results of shallow trenches.

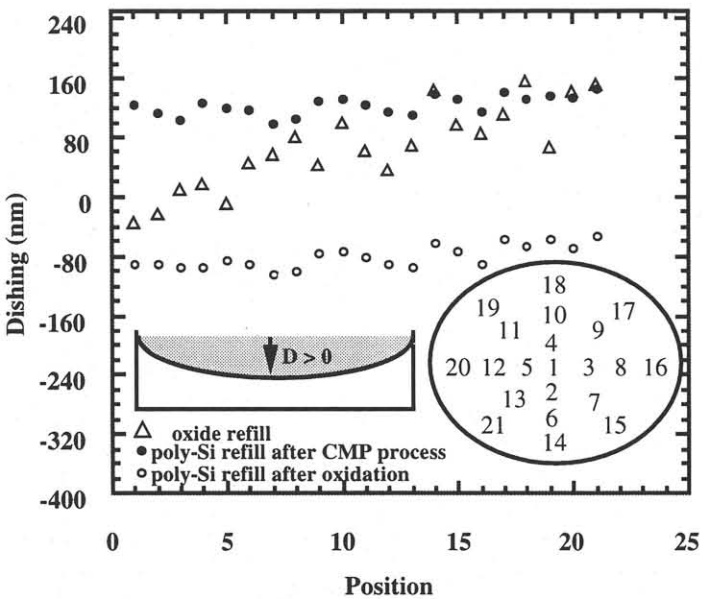


Fig. 5 The dishing distribution for 100-um wide field regions across 6-inch diameter wafers..

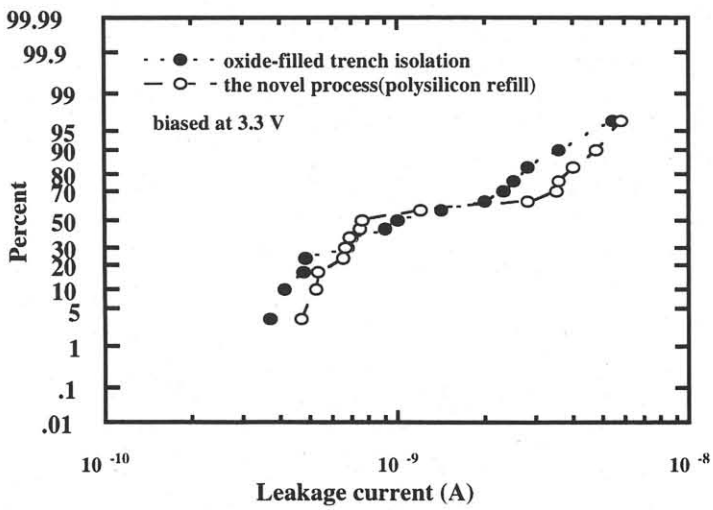


Fig. 6 The leakage current distribution of the n $^{+}$/p junction diodes.