Observation of Negative Differential Resistance Phenomena in Porous Silicon Superlattice Structures

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The current-voltage (I-V) characteristics of a porous Si (PS) superlattice (SL) structure based on n-type Si wafers fabricated via anodic etching under periodic ultraviolet (UV) illumination are reported and discussed. Strong negative differential resistance (NDR) phenomena were observed at room temperature in the proposed structure. The influence of the resistivity of the n-type Si wafer on the *I-V* characteristics, *i.e.*, either rectification or symmetry, is also presented. In addition, the dependence of peak-to-valley current ratio (PVCR) on the illumination condition is also investigated in this work.

1. Introduction

The superlattice (SL) structures with negative differential resistance (NDR) which caused by miniband transport was originally proposed by Esaki and Tsu.¹⁾ With inherent physics and potential applications for high speed devices, it has attracted much interest. However, most NDR devices are based on III-V or II-VI material systems, the studies on Si-based NDR devices are rarely reported. In this work, the observation of pronounced NDR phenomena on current-voltage (*I-V*) characteristics of a porous silicon (PS) SL structure is reported for the first time. The excellent performance of the proposed device might make possible the integration of functional NDR devices with well-developed Si technology.

The PS SL structure is a new type of Si-based heterostructure.²⁻⁵⁾ With the periodical variation of porosities (perpendicular to the surface of the wafer), a layered structure with a periodical change of bandgaps is expected^{6,7}) if the dimension of the nanocrystalline columnar structure is small enough (< 5 nm). In general, the PS SL structures can be divided into two categories called type I and type II according to the formation techniques.^{2,3}) Type I structure is usually obtained from homogeneously doped substrates with anodization etching parameters such as the current density or the illumination power being varied periodically during the anodization process.⁴⁾ Type II structure is formed on the substrates with periodical variation of doping concentration or mole composition, while the etching parameters are kept constant.2)

Frohnhoff *et al.* investigated both types of PS SLs via transmission electron microscopy (TEM).²⁾ Berger *et al.* applied the type I PS SLs to form highly reflective (99%) layer systems and Fabry-Perot filters.³⁾ In addition, a PS SL optical filter

device with very good characteristics was successfully fabricated by Vincent.⁴⁾ In this work, the *I-V* characteristics of a type I PS SL structure grown on n-type Si wafers were investigated for the first time. Pronounced NDR phenomena with either rectifying or symmetric characteristics, depending on the resistivity of the n-type wafer, were observed in the *I-V* curves. Also, the influence of the well thickness in SL on the peakto-valley ratio (PVCR) is studied in this work.

2. Experiments

The schematic sketch of the experimental setup for preparing PS samples in the study are shown in Fig. 1. A mixture of $HF:C_2H_5OH=1:4$ was utilized as the etching solvent here. The PS samples were prepared on two kinds of n-type Si (100) wafers, one with a high resistivity of 1~5 Ω cm (lightly doped) and one with a low resistivity of 0.01~0.1 Ω cm (heavily doped). The anodization etching current was supplied by an external constant current source which was kept at 20 mA/cm².

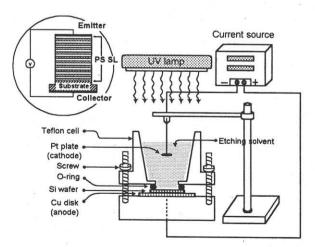
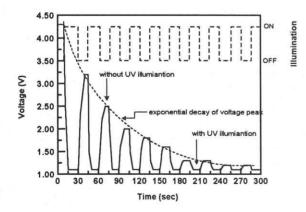
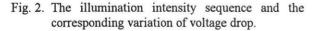


Fig. 1. The schematic sketch of the experimental setup.

An ultraviolet (UV) lamp of 750 µW/cm² with a wavelength of 365 nm was served as the illumination source during the etching process. It was programmed to switch on and off periodically so as to form the layered structures with different porosities. A typical 10-period illumination sequence with period time of 30 sec (15 sec dark and 15 sec illuminated) was shown in Fig. 2. In fact, a different dark half-cycle time would result in a different well width in SL. To study the influence of the well width on the PVCR, the dark half-cycle time of 15, 30, 45, and 60 sec were investigated. In addition, a conventional PS structure using a constant UV illumination during the anodic etching process was also fabricated for comparison.

In Fig. 2, the corresponding voltage drops between the anode and the cathode during the periodically illuminated etching process are also shown. The major factor affecting the voltage drop under a constant anodization current was found to be the intrinsic resistance between the anodized pore (trench) tip⁸⁾ and the bottom contact of the sample. Since a large amount of photo-induced electron-hole pairs are generated by the UV light illumination, the intrinsic resistance was relatively much smaller during the illumination half-cycle than that under dark condition. As a result, the measured voltages were kept at a low level (about 1.1 V). During the dark half-cycle, however, the electron-hole pairs diminish and the intrinsic resistance increases which results in the increase of voltage. An exponential decay of voltage peaks was found in the voltage-time characteristic. It is attributed to the thinning down of the wafer during the etching process, which results in the decrease of intrinsic resistance and hence voltage drop.





Once the PS SLs were formed, the samples were immediately metalized to form ohmic contact on the surface of the PS SLs. A shadow mask was used during the metalization via thermal evaporation. AuSb was adopted as the ohmic contact metal for the PS SLs, while the original Al contact on the back side of the wafer was retained to serve as another electrode. For electrical measurements, the Keithley 236 Source-Measure Unit (SMU) was employed.

3. Results and Discussions

Typical measured *I-V* characteristics at room temperature for the 10-period PS SL structures and conventional PS structures, both on high and low resistivity wafers, are shown in Figs. 3 and 4, respectively. Strong NDR phenomena were observed. Under forward bias, the onset of the NDR regions were found to be around 5.9 V and 2.4 V, the peak-to-valley current ratios (PVCRs) were of 3.3 and 2.6, respectively.

The *I-V* characteristics of the conventional PS structures were shown in the insets of Figs. 3 and 4 for comparison. No NDR phenomenon was observed from the conventional PS samples. It implies that the NDR phenomena are the results of the periodical variation of porosity. Since PS layers with different porisities behave as different material with different properties. It is thought that the periodical variation of porosity forms a periodical quantum well structure in which the higher (lower) porosity layer corresponds to the barrier (well) region as in conventional III-V quantum well heterostructures.⁶⁾ The observed NDR phenomenon might attribute to a miniband transmission analogous to the resonant transmission of light through a Fabry-Perot etalon.9) A detailed study on the transport mechanism of the PS SLs is now under way. These results will be published elsewhere.

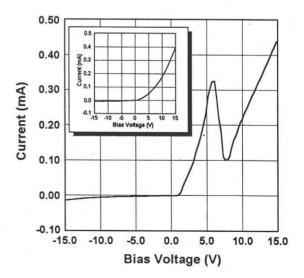


Fig. 3. The *I-V* characteristic of PS SL structure and conventional PS structure (shown in the inset) based on high resistivity wafers.

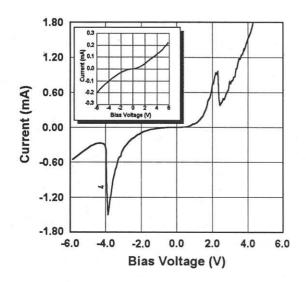


Fig. 4 The *I-V* characteristic of PS SL structure based on low resistivity wafers. Shown in the inset is the *I-V* characteristic of conventional PS structure.

Inspection of Figs. 3 and 4, rectifying characteristics were found in the lightly doped samples both in PS SL and conventional PS structures, however, the heavily doped samples show symmetric characteristics. The occurrence of the rectifying characteristics suggests the presence of a Schottky barrier in the metal/PS junction. The same phenomenon has also been pointed out by Beale *et al.*¹⁰) For the heavily doped samples the increased doping has made the barrier sufficiently narrow for tunneling to occur. Under such a situation, the rectifying characteristic disappeared.

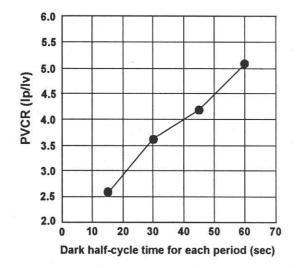


Fig. 5. Dependence of PVCR on dark half-cycle time for each period on high resistivity wafers.

In addition, the influences of well width, depending on the dark half-cycle time, on PVCRs are investigated, as shown in Fig. 5. The results suggest that a larger well width would result in a high PVCR. It is due to that the increase of well width lowers down the resonance level and hence increases the effective barrier height for electrons. This result is in accordance with that in the conventional III-V SL structure case.¹¹

4. Conclusions

In summary, a Si (n-type) PS SL structure fabricated by anodization etching under periodical illumination was UV proposed. The I-V characteristics of type I PS SLs were investigated and discussed for the first time. Strong NDR phenomena were observed at room temperature for PS SL structure. On the contrary, the conventional PS samples show no NDR phenomenon. It is also found that both PS SL and conventional PS structures grown on high resistivity n-type Si wafers give rise to rectifying I-V characteristics, while symmetric I-V characteristics were obtained from low resistivity wafers. In addition, the preliminary experimental results also indicate that larger well width can improve the PVCR of the proposed device.

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