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Smart-Cut: A New S.O.I. Material Technology Based on Hydrogen Implantation and Wafer Bonding

MICHEL BRUEL, Bernard ASPAR
LETI/CEA Département de Microtechnologies
CEA Grenoble - 17 rue des Martyrs - 38054 Grenoble Cedex 9 - France

André-Jacques AUBERTON-HERVE
SOITEC
Site Technologique ASTEC - 15 rue des Martyrs - 38054 Grenoble Cedex 9 - France

1. ABSTRACT

An alternative route to existing S.O.I. Material Technologies such as SIMOX and BESOI[1] is the new SMART-CUT® process, involving two technologies : wafer bonding and ion implantation. Implantation enables a high uniformity of the top silicon layer ; wafer bonding enables the original crystal quality of the bulk silicon to be kept. Details of the Smart-Cut® process and physical phenomena involved in the different technological steps are discussed. Thickness homogeneity, crystalline defects, surface microroughness, and electrical characterization of the UNIBOND SOI wafers obtained by means of the SMART-CUT® process, are presented.

2. THE SMART-CUT PROCESS

Smart-Cut [2] uses commercially available (100) silicon wafers with standard specifications as starting material; it basically comprises four main steps (Fig. 1).

Step 1. Wafer A is capped (Step 1-a) with a dielectric layer, thermally grown SiO_2 for example, this dielectric layer becoming the buried oxide of the SOI structure. Hydrogen ions are then implanted (dose in the $3.5x10^{16}$ to $1x10^{17}$ cm^{-2} range) into wafer A (Step 1-b).

Step 2. Hydrophilic bonding at room temperature of wafer A to a handling wafer B (wafer B is either bare or capped). Both wafers are previously cleaned using a modified RCA process. Wafer B plays a key role in the Smart-Cut process as a stiffener and provides the bulk silicon under the buried oxide in the SOI structure.

Step 3. Two-phase heat treatment of the two bonded wafers. During the first phase (400-600°C) the implanted wafer A splits into two parts : a thin layer of monocrystalline silicon remaining bonded to wafer B thus giving rise to a SOI structure, and the remainder of wafer A. The second high temperature treatment phase (around 1100°C) strengthens the chemical bonds.

Step 4. Touch polishing - after splitting, the layer of the SOI structure exhibits microroughness (Fig. 2) which makes polishing (Step 4-a) of the surface necessary.

Noteworthy : Wafer A whose surface layers (Si + SiO_2) were removed by the splitting process, can be recycled using a touch polishing (Step 4-b) to be used as wafer B in a subsequent process flow.

The Smart-Cut process is a generic process as described in [3] and applies to other Semiconductors (for example SiC [4]), other substrates (Silicon on glass or quartz) and also for transfer of structured and patterned layers or even active layers of electronic devices.

3. PHYSICAL ASPECTS RELATED TO HYDROGEN IMPLANTATION

Implantation of hydrogen in silicon at high dose ($>1.5x10^{17}$ cm^{-2}) induces formation of blisters at the surface (fig.3). This phenomenon can also be obtained for lower implantation doses ($\approx$ a few 10^{16} to 10^{17} cm^{-2}) when followed by thermal treatment at a medium range temperature (400°C to 600°C). The originality of the Smart-Cut® process is to use the basic physical phenomenon related to blistering, i.e. creation of microcavities containing a gas phase, as a way of inducing an in-depth splitting at the end of the range of implanted protons over the whole wafer.

In the Smart-Cut® process, the handling wafer is bonded with the implanted wafer and acts both as a stiffener and as a support for the transferred layer. The stiffener plays a key role in the splitting phenomenon; in the case of poor bonding of the two wafers splitting does not occur. Using TEM microscopy cross-sections, microcavities located at the depth of the projected range were observed. The mean size of these microcavities increases during annealing, and these cavities interact during the annealing step, resulting in the propagation of a crack parallel to the bonded surface (fig. 4). Cavities are not only located in one atomic plane but in a layer the thickness of which corresponds to the ΔRp (projected range straggling). So after splitting, a high degree of surface microroughness is obtained (12 nm RMS) (fig. 2).

4. CLEANING AND BONDING

To achieve high quality bonding, the contacting wafers must be scratch-free and cleaned to remove any particle or organic contamination. Microroughness also influences the bonding and must be lower [5] than 0.5 nm RMS. To form the SOI wafer, hydrophilic conditions are used to bond the implanted oxidized wafer to the silicon handling substrate.

The Smart-Cut® process requires specific cleaning conditions before bonding because the implantation step modifies the oxide surface in terms of particle contamination and organic pollution. The particle contamination is measured using a 6200 Tencor Surfscan; organic surface contamination is identified as hydrocarbon contamination using MIR-FTIR spectroscopy.

In the case of unoptimized cleaning, macroscopic defects can be detected just after the first annealing step, i.e. the splitting step.

Untransferred zones : large particles induce an unbonded area, resulting in an effective local lack of stiffening effect, thus preventing the splitting phenomenon from occurring in this area.

Microvoids : Particle and hydrocarbon pollution induce microvoid formation at the bonding interface. These small defects tend to inflate as soon as the splitting phenomenon occurs, resulting in a plastic deformation of the SOI surface.

In order to avoid formation of such defects, a special cleaning procedure using a modified RCA process was developed. After implantation, the bonding ability of the oxide surface is restored, almost no particle of a size larger than 0.3 µm is trapped between the wafers at bonding; the bonding sites density (OH-groups) is rather high, resulting in a fast bonding wave velocity evaluated to be in the range of several cm/S using IR transmission observation. This specific cleaning gives a final SOI structure free from macroscopic defects, as revealed by magic mirror view observation (Hologenix equipment / fig.5).

5. CHARACTERIZATION OF THE SOI STRUCTURE

The SOI structure exhibits uniformity of the silicon layer thickness better than 10 nm min-max over 100 mm wafers. For the surface microroughness, results comparable to bulk substrates are obtained with microroughness lower than 0.15 nm RMS.

To assess the crystalline quality of the silicon layer, chemical characterization was carried out using a four-step Secco etch. A density of etch pits ranging from 10^3 to several 10^4 /cm^2 was measured for 50 nm of silicon remaining after the first etch. SEM observations of the etch pits showed an unconventional shape for crystal defects. The origin of such defects is still unknown and a study is underway to check on whether the starting silicon substrates exhibit these defects. To check the density of defects threading through the SOI layer, epitaxy was performed on the SOI wafer. A Secco etch on this epitaxied structure showed a very low defect density of about 20 defects/cm^2, identified as threading dislocations through the SOI layer. No stacking faults or slip lines were observed over wafers both before and after epitaxy demonstrating a very high crystal quality of the final SOI material. Moreover, a 50% HF solution etch during 15 mn revealed a density of etch pits of about 1/cm^2.

The electrical behavior of the SOI structure was evaluated using a pseudo-MOS transistor [6]. The doping of the silicon film is p-type and was measured at 5.10^{15}/cm^3. Interface state densities and mobilities were found to be as good as for the best S.O.I. Materials.

ULSI electronic devices made with ultra-thin gate oxides (4 nm) have demonstrated interesting electrical behavior with extremely low defect densities. The breakdown intrinsic field was measured at about 15 MV/cm both on SOI wafers and best silicon materials. I-V measurements on capacitors of various sizes show that no pinhole or conductive defects exist in the buried oxide of the Unibond wafers.

6. CONCLUSION

The Smart-Cut process appears to be highly suitable for making high-quality SOI wafers with the great advantages, related to the intrinsic properties of light ion implantation, of low defect density and thickness homogeneity. All the basic steps involved can be performed on standard microelectronics equipment. Unlike BESOI technologies, no wafers are wasted in any grinding and thinning operations; a single bulk silicon wafer is required to achieve an SOI wafer. The Smart-Cut process could hopefully be the way to a less expensive but high-quality SOI material giving rise to a rapidly increasing breakthrough of SOI technologies into the advanced mass production market.

References

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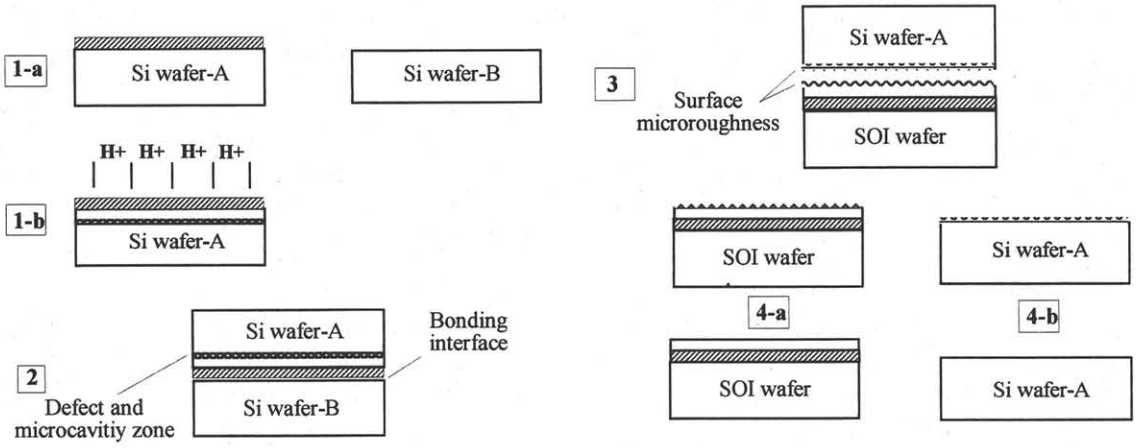


Figure 1: Schematic of the Smart-Cut® process

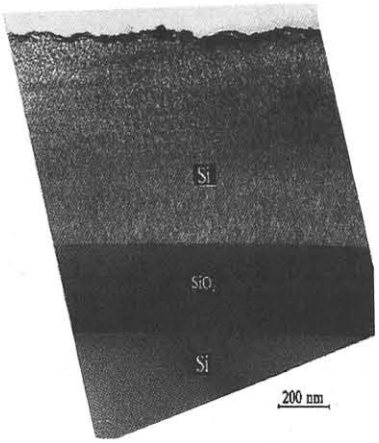
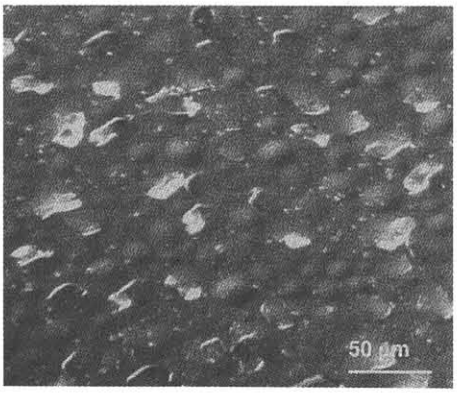


Figure 2 : TEM cross-section observation of the surface morphology after splitting.



Figures 3 : Blistering and flaking induced by high dose hydrogen implantation into silicon.

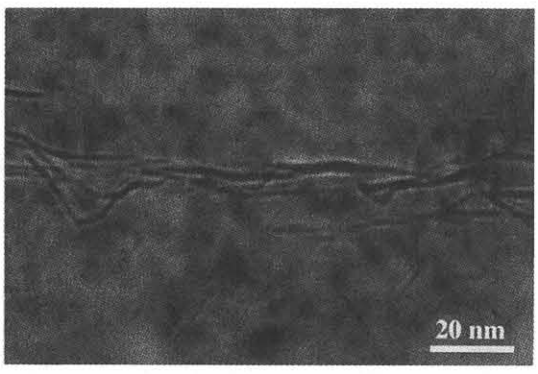


Figure 4: High resolution TEM cross-section observation of microcavities generated by a 3.10^{16}H+/cm² implantation at 95 keV and subsequent annealing (500°C, 30 min) with a bonded stiffener.

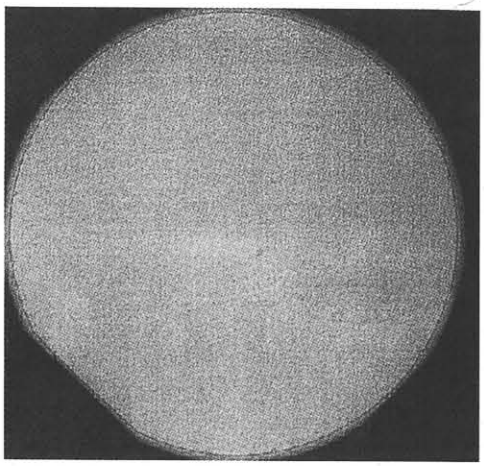


Figure 5: Magic mirror views of SOI structures after splitting for an improved cleaning.