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# Velocity Overshoot and $G_m$ Limitation in sub-0.1$\mu$m Fully-Depleted SOI-MOSFETs

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We have experimentally investigated the carrier velocity overshoot and the mechanism for the velocity degradation in fully-depleted SOI-MOSFETs. It is shown that, in sub-0.1$\mu$m SOI-nMOSFET, the velocity overshoot greater than $1\times10^7$ cm/s is realized at room temperature when the gate bias is low. The velocity degradation due to the self-heating effects is found to be smaller than the degradation caused by the increase of the vertical field. Moreover, it is suggested that the velocity degradation is also caused by the carrier-carrier scattering at high gate drive in addition to the above degradation mechanism. Consequently, in sub-0.1$\mu$m SOI-nMOSFETs, the transconductance can be improved by the velocity overshoot for a low supply voltage.

## 1 Introduction

To get a higher current drive in less than 0.1$\mu$m MOSFETs, it is very important to achieve a velocity overshoot exceeding $1\times10^7$ cm/s at the source edge. In our previous work [1], we have shown the possibility of the velocity overshoot in fully depleted sub-0.1$\mu$m SOI nMOSFETs, when the self-heating effects are suppressed.

In this study, we have experimentally verified that the velocity overshoot at the source edge can be realized in 0.08$\mu$m fully depleted nMOSFETs at room temperature in the low gate bias region, where the self-heating is suppressed. Based on the experimental results, we have quantitatively clarified the physical mechanism of the carrier velocity degradation.

## 2 Experimental

0.08$\mu$m fully depleted SOI CMOS devices were fabricated on SIMOX wafers. The gate-electrode was patterned by EB lithography. The gate oxide thickness was 44Å, and the buried oxide thickness was 1000Å. The SOI layer thickness was 400Å. The Ni silicide structure was formed, and the source/drain parasitic resistances were very low ($\sim$300 $\Omega\cdot\mu$m) in spite of thin SOI. The channel mobility was very high due to the low impurity concentrations. The peak values of mobility were 820 and 200 $cm^2/V\cdot s$ for electron and hole, respectively.

## 3 Results and Discussion

### A. Velocity Overshoot

In this study, we obtained the carrier velocity near the source by $v(V_g) = G_m(V_g)/C_{gs}(V_g)$, where $G_m$ is the measured transconductance and $C_{gs}$ is the gate-to-source capacitance [2]. We can investigate the carrier velocity in the self-heating free condition, that is in $V_G \sim V_{TH}$. Figure 1 shows $C_{gs}$ and $G_m$ and the gate-to-drain capacitance $C_{gd}$ of 0.08$\mu$m SOI-nMOSFET at Vd=1V. The inset shows the lattice temperature $T_L$ obtained by the gate electrode resistance method [3]. $G_m$ is very large ($G_{m\ max}$=600mS/mm) owing to the low S/D resistance. The capacitance characteristics are almost the same as those of the long channel devices, and indicate the existence of the pinch-off region even in sub-0.1$\mu$m MOSFETs [2].

Figure 2 shows the carrier velocity $v = G_m/C_{gs}$ in 0.08 and 0.1 $\mu$m SOI-MOSFETs. It should be noted that, in $L_{eff} = 0.08\mu$m, the electron velocity exceeds $v_{sat} = 1\times10^7$ cm/s ($\sim1.2\times10^7$ cm/s) in $V_g \sim V_{th}$, i.e. the self-heating free conditions. This clearly shows that the velocity overshoot can be realized in sub-0.1$\mu$m fully depleted SOI-nMOSFET when the gate bias is low, whereas the velocity overshoot is not observed in $L_{eff} = 0.1\mu$m, as shown in Fig.2(b). Moreover, the electron velocities are almost independent of $V_d$ in Fig.2, and this means the pinch-off potential is not affected by $V_d$. On the other hand, the maximum hole velocity is at most $6.4\times10^6$ cm/s in $L_{eff} = 0.08\mu$m at $V_d$=-1.5V and is about 60 % of the electron velocity. This is because hole effective mass is greater than that of electron.

### B. Velocity Degradation Mechanism

In this section, we introduce the intrinsic velocity, $v_i$ obtained by the intrinsic $G_m$ considered

the source/drain parasitic resistance. As shown in Fig.2, $\upsilon$ degrades in the higher $V_G$ region. To elucidate the mechanism of the degradation, we experimentally investigated the lattice temperature $T_L$ and the vertical electric field $E_{eff}$ dependence of $\upsilon_i$. Figure 3(a) shows the experimental data of $T_L$ dependence of the intrinsic $\upsilon_i$ obtained in 0.13$\mu$m bulk-MOSFETs by using the hot chuck. The velocity degradation in Fig.3(a) is due to the mobility reduction caused by the increase of $T_L$. We obtain $\upsilon_i \propto T_L^{-0.78}$ for $L_{eff} = 0.13\mu$m by the power curve fit. Figure 3(b) shows $E_{eff}$ dependence of $\upsilon_i$ translated from the experimental data of $V_{SUB}$ dependence of $\upsilon_i$ in 0.08 and 0.13$\mu$m SOI-nMOSFETs. The degradation in Fig.3(b) is due to the mobility reduction caused by the increase of $E_{eff}$. We find $\upsilon_i \propto E_{eff}^{-0.11}$ for $L_{eff} = 0.13\mu$m by the power curve fit. For the $T_L$ and $E_{eff}$ dependence, we have obtained almost the same power laws in all ranges of the gate drive, that is both the phonon and the roughness scattering regions.

Using these power laws, the electron velocity degradation is estimated for 0.13$\mu$m SOI-nMOSFET, as shown in Fig.4. Figure 4(a) shows the velocity degradation at $V_{SUB} = 0$V. The velocity degradation due to the self-heating is found to be smaller than that caused by the increase of $E_{eff}$. For low gate drive, $\upsilon_i$ degradation can be explained by both $T_L$ and $E_{eff}$ dependence of $\upsilon_i$, as shown as the open circles in Fig.4(a). However, notice that the degradation of the intrinsic $\upsilon_i$ is larger than the degradation caused by both the self-heating and the increase of $E_{eff}$. This indicates that some anomalous scattering degrades the velocity. Note that the discrepancy becomes larger at higher $V_G$. This discrepancy is also enhanced at applied $V_{SUB}$, as shown in Fig.4(b). Since each of the $V_G$ and $V_{SUB}$ applications increases the electron concentration per unit volume in the inversion layer, these suggest that the carrier-carrier scattering degrades the velocity [4].

Figure 5 shows the estimated components of the velocity degradation in 0.13$\mu$m SOI-nMOSFET at $V_G - T_{TH} = 0.8V$. It is shown very clearly that the degradation by some anomalous scattering, maybe e-e scattering, increases monotonically with the application of $V_{SUB}$, whereas both the $T_L$ and $E_{eff}$ dependence of the degradation is almost constant.

Figure 6 shows the estimated components of $\upsilon_i$ degradation for 0.08$\mu$m SOI-nMOSFETs in which the velocity overshoot is observed. We find that $\upsilon_i$ at $V_G - V_{TH}$=1.65V degrades remarkably down to 58% of that at $V_G - V_{TH}$=0V. In shorter $L_{eff}$, the self-heating effects are more remarkable. However, in Fig.6, the degradation caused by the self-heating is still small and about one-third of the total $\upsilon_i$ degradation. The other two-thirds of the total degradation consists of the degradation components of $E_{eff}$ and e-e scattering, which are not characteristic of the SOI structure but general for MOSFET. The $E_{eff}$ and e-e scattering components increase greatly with $V_G$. This indicates, in a high $V_G$ region, there will be no remarkable improvement in the transconductance even if the self-heating is suppressed completely. Since, however,in the future, low power performance will be a main application of MOSFETs, the velocity degradation components at high $V_G$ will not be a serious problem. Therefore, in sub-0.1$\mu$m SOI-nMOSFETs, the velocity overshoot is very useful for high performance at a low supply voltage.

## 4 Conclusion

We have experimentally studied the carrier velocity $\upsilon = G_m/C_{gs}$ and the velocity degradation mechanism in fully depleted SOI-MOSFETs. We found that, at low $V_G$, the velocity overshoot over $1\times10^7$ cm/s is realized at room temperature. Moreover, it was experimentally shown that the velocity is restricted not only by the increase of both $T_L$ and $E_{eff}$ but also by another mechanism, perhaps, carrier-carrier scattering. Since the velocity restriction increases remarkably with $V_G$, a higher $G_m$ will be not realized at large $V_G$ by using the velocity overshoot effect, even if the self-heating is suppressed completely. However, MOSFETs will be used at low supply voltage more and more in the future. Hence, under the low voltage conditions, we can expect a high performance owing to the velocity overshoot effect in sub-0.1$\mu$m SOI-nMOSFETs.


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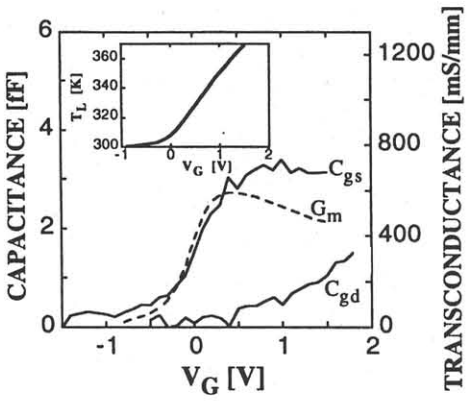


**Fig.1** Gate-to-source capacitance $C_{gs}$, gate-to-drain capacitance $C_{gd}$ and measured transconductance $G_m$ vs. $V_G$ in $L_{eff}/W_{eff} = 0.08/10\mu m$ SOI-nMOSFET, where $V_D = 1V$, $V_{sub} = -8.5V$ and $T_{SOI} = 400Å$. The inset shows the lattice temperature $T_L$ raised by the self-heating as a function of $V_G$.

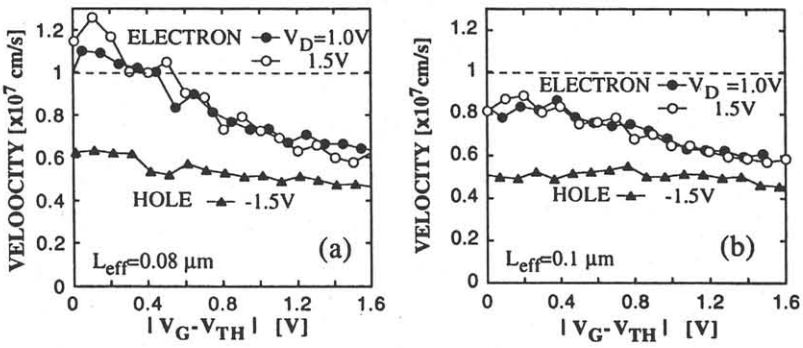


**Fig.2** Carrier velocity $v$ vs. $| V_G - V_{TH} |$, where $T_{SOI} = 400Å$, $| V_{SUB} | = 8.5V$. (a) Carrier velocity in $L_{eff} = 0.08\mu m$. Electron velocity exceeds $1 \times 10^7$ cm/s near $V_{TH}$. (b) The carrier velocity in $L_{eff} = 0.1\mu m$.

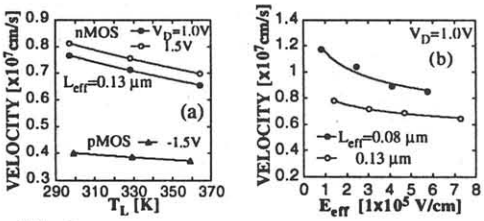


**Fig.3**
(a) Intrinsic carrier velocity $v_i$ degradation as a function of $T_L$ in bulk-MOSFETs. The velocity is obtained for 0.13$\mu$m bulk-MOSFETs at the same $V_G - V_{TH}$.(b) Intrinsic carrier velocity $v_i$ degradation as a function of $E_{eff}$ in 0.08$\mu$m and 0.13$\mu$m SOI-nMOSFETs. $E_{eff}$ is calculated by the one dimensional model as a function of $V_{SUB}$ and $V_G - V_{TH}$. The velocity is obtained at the same $V_G - V_{TH}$ ($\sim 0.1V$).

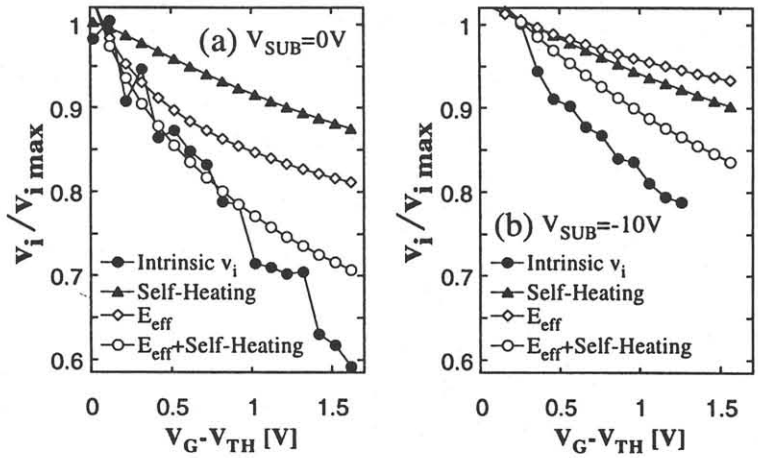


**Fig.4** Intrinsic electron velocity degradation mechanism in 0.13$\mu$m SOI-nMOSFET at $V_D = 1V$. The intrinsic $v_i$ is obtained by $v_i = G_{in}/C_{gs}$, where $G_{in}$ is the intrinsic transconductance. $v_i$ degradation is compared with the degradation due to the self-heating only, the degradation due to the $E_{eff}$ increase only and the degradation due to both the self-heating and the $E_{eff}$ increase. (a) $V_{SUB} = 0V$, and $v_{i\,max} = 8.5 \times 10^6$ cm/s. (b) $V_{SUB} = -10V$, and $v_{i\,max} = 7.1 \times 10^6$ cm/s.

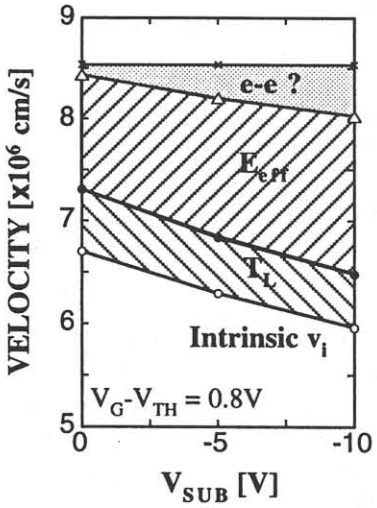


**Fig.5** $V_{SUB}$ dependence of the estimated components of the velocity degradation in 0.13$\mu$m SOI-nMOSFET at $V_D = 1V$. $v_i$ degradation at applied $V_{SUB}$ is compared with that at $V_{SUB} = 0V$.

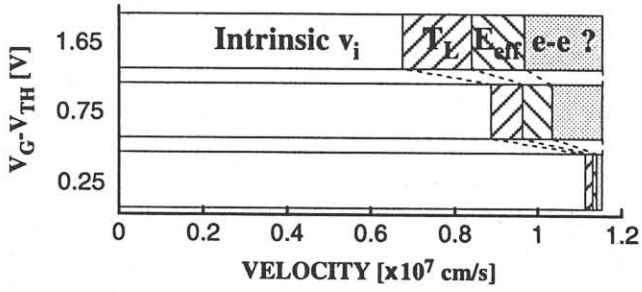


**Fig.6** Gate drive dependence of the estimated components of electron velocity degradation in 0.08$\mu$m SOI-nMOSFET. $v_i$ degradation at applied $(V_G - V_{TH})$ is compared with that at $(V_G - V_{TH}) = 0V$.