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New Electrically-Thinned Intrinsic-Channel SOI MOSFET with 0.01μm Channel Length

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In the ultra small device with the channel length of 0.01μm, only one impurity atom on the average exists in the channel region even though the impurity concentration is higher than $5.0\text{x}10^{18}\text{cm}^{-3}$. Therefore, the device characteristics significantly change from device to device within a wafer or even within a chip due to the statistical variation of the impurity concentration. Then, we have investigated the influences of isolated atoms in the channel region on the device characteristics based on Monte Carlo simulation and proposed a new 0.01μm SOI MOSFET with no channel doping to suppress the influences of statistical variation and the short channel effect.

1. Introduction

To scale-down the device size has been the most effective way to improve the performance and to increase the packing density in LSIs. The device size has been already scaled-down beyond 0.1μm in the research and many sub-0.1μm devices have been reported so far[1,2]. It has been also reported that the device performance continues to be improved with scaling the device size down to 0.04μm in the gate length of MOSFET and the short channel effect can be suppressed considerably well even in such small size device[3]. In this paper, we discuss the possibility of further scaling the device size down to 0.01μm based on the Monte Carlo simulation and the hydrodynamic simulation focusing on the short channel effect and the influences of the statistical variation of impurity concentration.

2. Concerns of Conventional Device Scaling

In order to examine the possibility of employing the conventional device scaling-down method in 0.01μm resume, the device characteristics of SOI MOSFETs as shown in Fig.1 are simulated at the first. The Monte Carlo simulation results for the electron distribution and the potential contour map of 0.01μm single gate SOI MOSFET with n^+-poly-Si gate are shown in Fig.2. The channel doping is increased to $5\text{x}10^{18}\text{cm}^{-3}$ in this device in order to suppress the short channel effect according to the conventional device scaling method. The Si substrate doping is $1\text{x}10^{16}\text{cm}^{-3}$. The effective gate oxide thickness is 2nm which can be realized by using the thin insulator with larger dielectric constant. SOI film thickness is 10nm. The drain voltage is 1V. Both results for the effective buried oxide thickness of 50nm and that for 2nm are shown in Fig.2. As is obvious in Fig.2 (a), the short channel effect becomes very significant when the buried oxide is thick because the drain electric field can easily penetrate into the channel region through the buried oxide. Therefore, it is very important to decrease the effective buried oxide thickness in order to suppress the

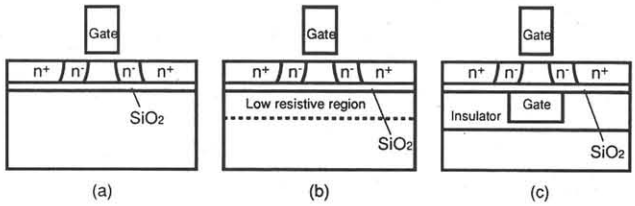
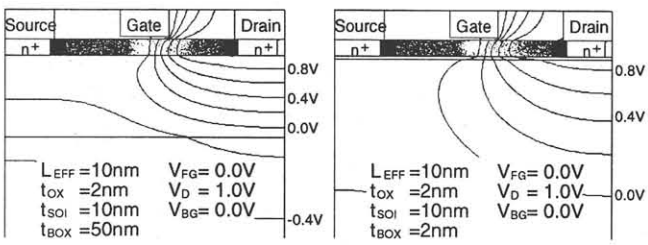


Fig.1 Cross-sectional view of SOI MOSFET (a),(b):single gate (SG) (c):double gate (DG) or single gate (SG) with back gate electrode



(a) t_{BOX} = 50nm (b) t_{BOX} = 2nm

Fig.2 Electron distribution and potential contour map in 0.01μm single gate SOI MOSFET with n^+-poly-Si gate

short channel effect. However, as is obvious in Fig.2 (b), the short channel effect can not be sufficiently suppressed even if the buried oxide thickness is reduced as long as the Si substrate with relatively low impurity doping is employed. This is because the drain electric field can penetrate into the channel region through the Si substrate. Therefore, the surface impurity concentration of Si substrate has to be increased. The I_D-V_D characteristics of such 0.01μm SOI MOSFETs obtained by the hydrodynamic simulation are shown in Fig.3 where both characteristics of the single gate device (SG) and the double gate device (DG) are plotted. The channel width is 1μm. The buried oxide thickness is 2nm. The surface impurity concentration of the Si substrate is $5\text{x}10^{18}\text{cm}^{-3}$. The depth of this high impurity concentration region is 20nm and the impurity concentration in the deeper region is $1\text{x}10^{16}\text{cm}^{-3}$. As is obvious from Fig.3, fairly good I_D-V_D characteristics are obtained by decreasing the buried oxide thickness and increasing the

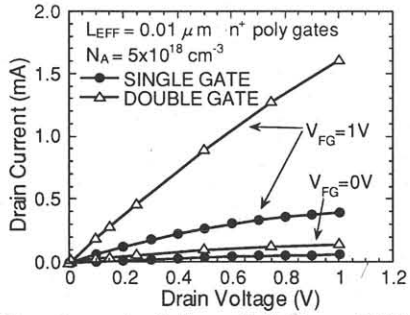


Fig.3 I_D-V_D characteristics of 0.01μm SOI MOSFET with channel doping

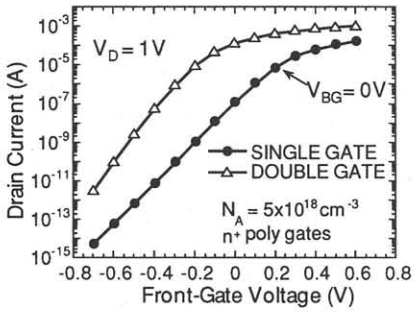
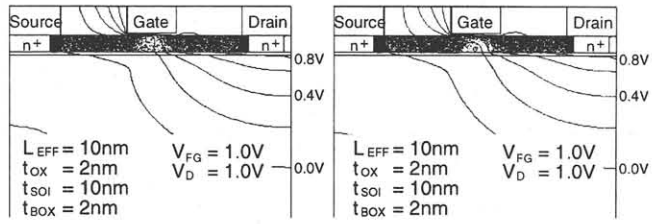


Fig.4 log I_D-V_{FG} characteristics of 0.01μm SOI MOSFET with channel doping

surface impurity concentration in the Si substrate. However, considerably large cut-off currents still flow at the gate voltage of 0V for both device structures as is obvious in Fig.4. The channel doping should be increased more to reduce the cut-off currents. However, the channel impurity concentration is already very high and hence can not be increased further. This means that the short channel effect can not be suppressed any more by using the conventional scaling-down method. In addition, the statistical variation of impurity concentration is another big problem in such small devices because only one impurity atom exists between the source and the drain even if the impurity concentration in the channel region is sufficiently high such as 5x10^{18}cm^{-3}. Then, the influences of the statistical variation of the impurity concentration was evaluated by adding one or zero impurity atom into the non-doped channel region in Monte Carlo simulation.

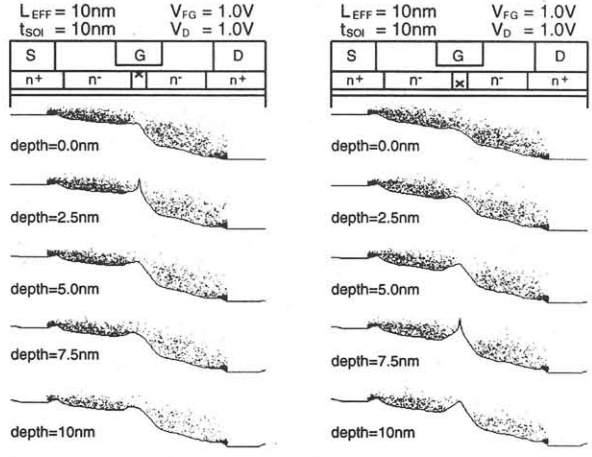
3. Influences of Isolated Impurity Atom in Channel Region

Figure 5 indicates the influence of the position of impurity atom on the electron distribution and the potential contour map in 0.01μm single gate SOI MOSFET. It is obvious in the figure that less electrons flow near the front interface when the impurity atom exists near the front interface than when it exists near the back interface. Therefore, the overall channel current is decreased. The influence of the position of impurity atom is more clearly represented in Fig.6 where the electron population in the conduction band and the potential distribution along the channel direction are plotted changing the depth from the front interface. It is clearly shown in the figure that the potential barrier is formed around the position where the the impurity atom exists. The variation of drain current by changing the position of impurity



(a) impurity atom near the front interface (b) impurity atom near the back interface

Fig.5 Influence of the position of impurity atom on electron distribution and potential contour map in 0.01μm single gate SOI MOSFET



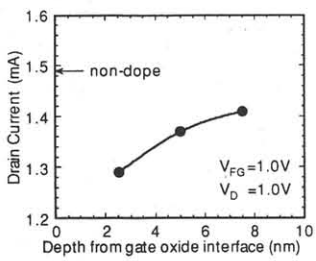
(a) impurity atom near the front interface (b) impurity atom near the back interface

Fig.6 Influence of the position of impurity atom on the potential distribution and the electron population in the conduction band along the channel direction changing the depth from the front interface
(n^-:1x10^{19}cm^{-3}, n^+:1x10^{20}cm^{-3})

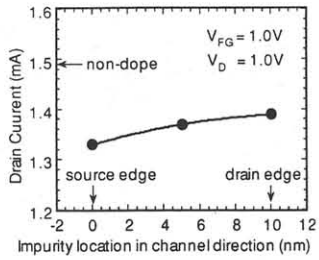
atom is shown in Fig.7. The drain current increases as the position of impurity atom shifts from the front interface to the back interface and from the source edge to the drain edge. In addition, the significant increase of the drain current is observed when the impurity atom does not exist in the channel region. Thus, the drain current significantly varies among the devices due to the statistical variation of impurity atoms.

4. New Scaling-Down Method and ETIC-SOI MOSFET

As is obvious from the previous discussion, the method to control the threshold voltage by changing the impurity concentration in the channel region can not be used in the 0.01μm resume. Therefore, non-doping in the channel region is more preferable in 0.01μm device. Furthermore, it is more effective to control the threshold voltage by applying the negative bias voltage to the Si substrate in the device structure shown in Fig.1 (b) or to the back gate electrode in the device structure shown in Fig.1 (c). These devices are single gate SOI MOSFET in operation because the voltage applied to the silicon substrate or the back gate electrode is fixed at a constant value. The



(a) changing the depth from the front interface



(b) changing the position from the source along the channel direction

Fig.7 Influence of the position of impurity atom on the drain current

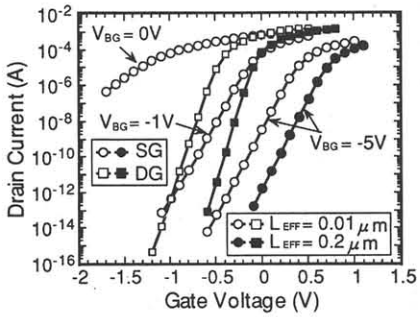


Fig.8 log I_D-V_{FG} characteristics of SOI MOSFET with no channel doping

subthreshold characteristics of single gate SOI MOSFET with the back gate electrode are plotted in Fig.8 where the characteristics for two kinds of channel lengths are shown. The characteristics for the double gate SOI MOSFET are also plotted in the figure for the comparison. The back gate bias voltage is changed as a parameter in the single gate SOI MOSFET in which n^+-poly-Si is utilized for the back gate electrode as well as the front gate electrode. It is clear in the figure that the subthreshold swing of the single gate SOI MOSFET is decreased by applying a negative voltage to the back gate electrode. In addition, it is also obvious in the figure that the cut-off current is significantly small in the single gate SOI MOSFET with the back gate bias voltage of -5V. The cut-off current can not be reduced in the double gate SOI MOSFET. Furthermore, it becomes clear by comparing the device characteristics of 0.01μm device with those of 0.2μm device that the difference of the threshold voltage is smaller and hence the short channel effect is less serious in the single gate SOI MOSFET with the back gate bias voltage of -5V than in the double gate SOI MOSFET. Therefore, 0.01μm device with excellent device characteristics can be achieved by using the single gate SOI MOSFET with a negative back gate bias voltage. The I_D-V_D characteristics of the 0.01μm single gate SOI MOSFET with the back gate bias voltage of -5V are shown in Fig.9. Excellent characteristics with large saturation current and small cut-off current are obtained. The reason why such excellent characteristics are obtained in the single gate SOI MOSFET with a negative bias voltage can be explained in Fig.10 where the electron distribution and the potential contour map of this device are shown. It is clear in the figure that electrons are pushed more closely to the front interface and the

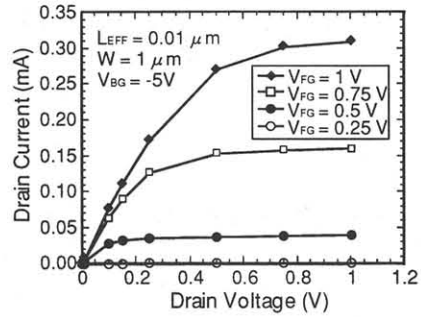


Fig.9 I_D-V_D characteristics of 0.01μm ETIC-SOI MOSFET

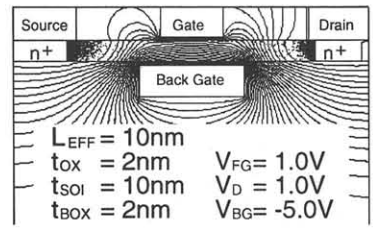


Fig.10 Electron distribution and potential contour map in 0.01μm ETIC-SOI MOSFET

equi-potential lines in the channel region are parallel to the interface. This means that the channel is electrically thinned by applying a negative bias voltage to the back gate electrode. It is not possible in the double gate SOI MOSFET to electrically thin the channel by applying the bias voltage. From the reason mentioned above, the short channel effect can be more effectively suppressed in the single gate SOI MOSFET with a negative back gate bias voltage. In addition, the variations of the device characteristics due to the statistical variation of the impurity atoms are not significant in this device because the impurity is not doped in the channel region. We call this device the electrically-thinned intrinsic-channel (ETIC) SOI MOSFET. Thus, it was shown that 0.01μm device with excellent device characteristics can be achieved using ETIC-SOI MOSFET.

5. Conclusion

It was shown based on the Monte Carlo simulation and the hydrodynamic simulation that 0.01μm device can not be achieved using the conventional device scaling-down method due to the significant short channel effect and the statistical variation of impurity atoms. We propose a new ETIC-SOI MOSFET with no channel doping to achieve the 0.01μm device with excellent device characteristics where the channel is electrically thinned by applying a negative back gate bias voltage.

References

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