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Vacuum Bonding for the Fabrication of PBSOI

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In order to fabricate PBSOI (Patterned and Bonded Silicon On Insulator), a specially designed vacuum bonding machine is introduced. This bonding machine has a self-controlled alignment mechanism (Rotating angle<0.01 ° , side margin<100um). In the bonding process, the roles of reduced pressure and interlayer films were experimentally proved to be effective for the surpression of particles and for the bondability of patterned wafers.

1. INTRODUCTION

The SOI technique based on wafer bonding has received increasing attention and recently, the technique extended to a novel process for high density SOI DRAM [1], which allowed to fabricate the cell capacitor completely buried under the thin silicon layer. The so-called technique, PBSOI, has several advantages, such as the merits of conventional SOI device, higher packing density and smaller backend topology. Meanwhile, the process for the fabrication of PBSOI requires starting conditions, which are the planarizing processes of patterned wafers to be able to directly bond to the handle wafers, and also the wafer to wafer alignment to accurately transfer patterns on patterned wafers to handle wafers. Even though the starting conditions to obtain such a process has been solved, the process is not still optimizing in terms of throughput and yield. The aim of this paper is to report the experimental results for the fabrication of PBSOI based on theoretical consideration.

2. EXPERIMENTAL

In order to fabricate PBSOI, we produced patterns, which were fabricated on 6 inch, p-type silicon wafer (thickness $675 \pm 15 \mu m$). The patterned wafer was first subjected to the fabrication of a polish stopper using a conventional LOCOS process and then the formation of the capacitors. Secondly, it requires several planarizing processes to be able to directly bond to the handle wafer. Finally, a reflow glass such as BPSG (3500Å) was deposited onto the patterned wafer and also handle wafer at 420℃ and flowed at 900℃ for 30min in nitrogen ambient in order to easily bond the two wafers. Bonding the two wafers was performed under reduced pressure (1mmTorr) at R.T by using a specially designed vacuum bonding machine. Subsequently the bonded wafers are annealed at 950℃ for 30min in nitrogen ambient. The backside of the patterned wafer in each pair was subsequently thinned down to 3.5 ± 1um using a precision grinder. In order to investigate the bonding interface the magic mirror method and IR imaging were used after the precision grinding. The ground wafer was dipped to polyetchant for 2min to remove mechanical surface damage and particles on ground surface. Finally a thin SOI device layer on capacitor was obtained after a selective CMP process [2] by using polish stoppers. The schematic procedure is shown in Fig. 1.

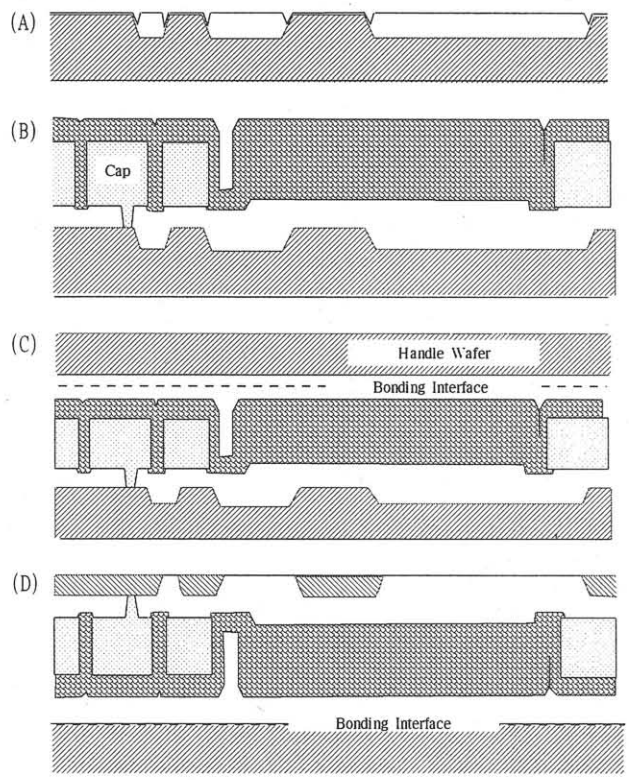

Fig.1: Schematic procedure of PBSOI: (a) Fabrication of stoppers using LOCOS process (b) Formation of Capacitor (c) bonding with handle wafer after planarization (d) Grinding and selective CMP.

3. RESULTS AND DISCUSSION

There are three requirements to be considered for the fabrication of PBSOI. One appears to correspond to the flatness of patterned wafers, which is closely related to the bondability of two wafers. In order to successfully bond the two wafers, the deposition of BPSG layer as an interlayer on both wafers are found to be helpful to prevent any voids at the bonding interface. When measuring the warpage and the surface roughness of the patterned wafer using an Capacitive probe and an AFM, the values are approximately 40um and 2Å, respectively. Without the reflow glass (BPSG) in the bonding process, it results in locally debonded areas, which might be from the wafer flatness of the patterned wafer. It is clear, when checking the bonding process in air atmosphere using IR imaging, that the propagation of bonding wave differs in each position of the wafer as described in Fig. 2.

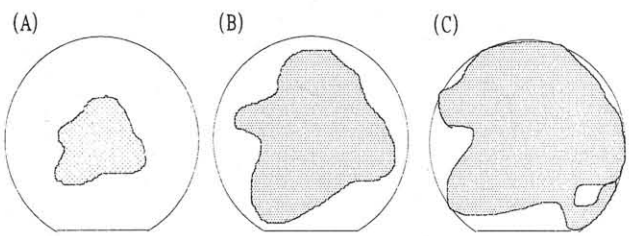

Fig. 2: The propagation behavior of a bonding wave for PBSOI. Due to the poor wafer flatness of patterned wafers the bonding velocity differs in each position and therefore locally debonded areas are generated.

In such a case, the trapped gas is finally separating the gas-trapped area of the bonded wafer after the grinding process. The reflow glass used in this bonding process consists of lower concentrations of B (2wt%) and P (4wt%). In our experiments, as the concentrations of B and P increase, the probability of void generation due to the precipitation of B&P related compound also increases with heat budget. Figure 3 shows an SEM image of the generation of voids inside the BPSG layer after heat treatments.

Another requirement is alignment accuracy in order to exactly transfer patterns onto handle wafers. Bonding must always occur within the speculation of rotating angle of <0.01 ° and side margin of <100um. Otherwise, a misalignment problem will occur in the successive lithography process. As shown in Fig. 4, a specially designed vacuum bonding machine shows a function of self -controlled alignment, which consists of side aligner and self-controlled roller.

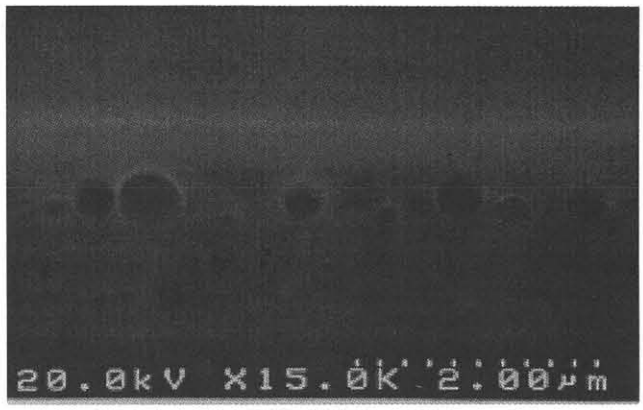

Fig.3: SEM image of voids generated inside BPSG layer after heat treatment. The voids are due to the precipitation of B&P related compound and mainly appeared in the case of higher concentrations of B&P

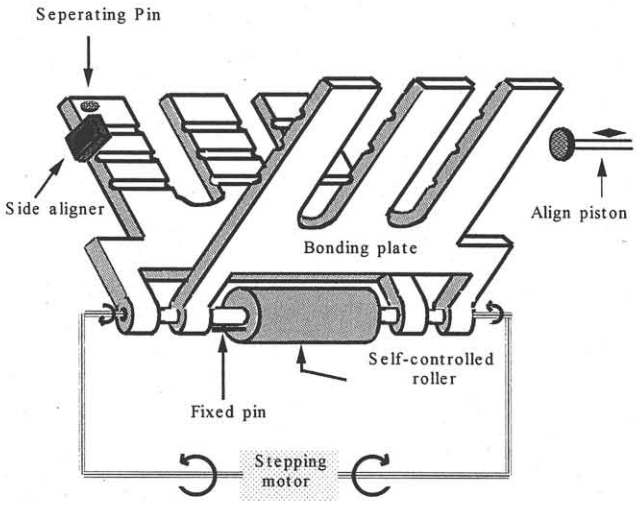

Fig.4: A specially designed vacuum bonding machine with spec. of rotating angle of<0.01 ° , side margin of<100um

When using the vacuum bonding machine, a patterned wafer can be successfully and automatically transferred to a handle wafer. Unfortunately, the two unexpected types of voids (See Fig. 5) at the bonding interface unlike during bonding in air atmosphere occurred, one of which is due to the oil backstream from the vacuum pump and the other one might be from volatile organic contamination coming from the chamber wall during pumping.

However, the undesirable voids can be easily prevented after changing a mechanical pump to an oil free pump, and after heating the vacuum chamber at 200℃ for 2 days.

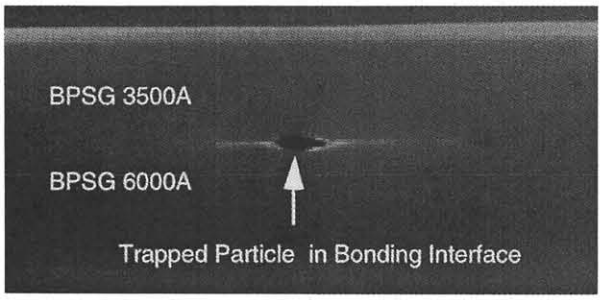

Fig.5: SEM image of trapped particle at bonding interface. Bonding was performed at reduced pressure (1mmTorr) and BPSG flow and annealing temperatures are 900 and 950℃, respectively

Bonding the two wafers under reduced pressure (1mmTorr) is required. Since propagation of the bonding wave is inversely proportional to pressure when bonding for hydrophilic surface as mentioned in Ref. [3,4] no time is allowable to generate gas-trapped areas due to the different bonding velocities in each positions of the wafer during the vacuum bonding process, and also only little gas remained in the vacuum chamber. Therefore, vacuum bonding will be very helpful for avoiding gas-trapped areas at the bonding interface. Another effect of reduced pressure in the bonding process is the surpression of trapped particles at the bonding interface by controlling the process parameters as shown in Fig. 5. The detailed explanation is based on theoretical considerations of the bonding process as shown in Fig. 6.

Fig. 6 : When bonding occurs in air atmosphere, the remaining gas (N_2) after annealing prevents the BPSG reflow into the void surrounding the particle and finally separating the area after grinding

The reason is as follows: 1) As described in Fig. 6, when bonding two wafers in air, the trapped gas surrounding a particle contains approximately 80% nitrogen and 20% oxygen. During high temperature heat treatment, oxygen reacts with the surrounding wall and nitrogen still remains in the void. In that case, the remaining gas(N_2) prevents the BPSG reflow into the void surrounding the particle and finally results in a local debonded area. 2) When bonding the two wafers under reduced pressure, no trapped gas remains in the void surrounding a particle and BPSG is refilling the void during annealing. 3) In order to easily reflow the BPSG layer into the void during annealing, the annealing temperature of the bonded wafers is higher than the BPSG flow temperature before bonding occurs. Since capacitors do not properly operate in the case of annealing over 1000℃ [5] the best experimental result was obtained at a flow temperature of 900℃ and an annealing temperature of 950℃. From the experimental conditions explained above, we finally obtain a void free thin SOI device layer (1500±80Å) on buried capacitors. Figure 7 shows the SEM image of PBSOI with buried capacitors.

4. REFERENCES

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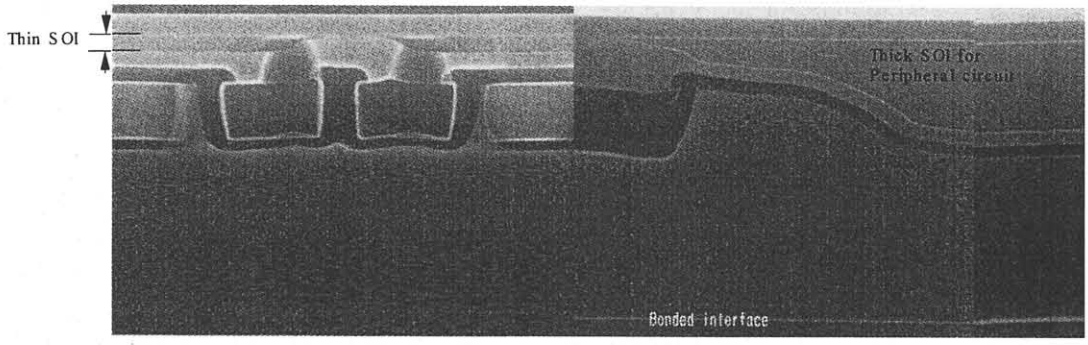

Fig.7: SEM image of PBSOI with buried capacitor