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Thin Film Silicon on Insulator Substrate Considerations for CMOS Technologies

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SIMOX and BSOI substrates have been obtained from SOI wafer suppliers over a period of 3 years. Material properties such as uniformity, defects, and contamination have been measured. In addition, MOS devices and capacitors have been fabricated on these substrates using a 0.5 μm CMOS flow. These results have been used to help improve the SOI substrate quality and to evaluate the production worthiness of SOI.

I. INTRODUCTION

For a number of years, silicon-on-insulator (SOI) substrates, devices, and circuits have been investigated. Before the 1990's, most of the work on SOI was exploratory or was for use in radiation hard applications and most of the substrates, devices, and circuits were custom crafted. During that time, the supply and quality of available substrates was low and the cost was high. However, because of the low demand and premium pricing on radiation hard parts, this was not a major obstacle.

In the early 1990's, however, many semiconductor companies recognized that circuits on SOI might finally be needed to meet the ever increasing demands for low power/low voltage, higher performance and higher packing densities than can not be easily achieved on bulk Si. This led a number of semiconductor companies to demand better quality, higher volume and lower prices from the SOI substrate manufacturers. For the IC manufacturer to produce a circuit with an acceptable yield and cost, it is necessary for the substrate suppliers to meet stringent quality, reproducibility, capacity and cost goals. Therefore, several companies have worked to meet these requirements by producing either SIMOX or thin film Si (<0.5 μm) bonded wafers (BSOI).

This paper will discuss our devices, gate oxide and material results on SIMOX and BSOI wafers. Substrates have been obtained from two SIMOX and two BSOI suppliers. The SIMOX process used by the two suppliers is very comparable and produces wafers with nominally 0.18-0.2 μm of Si over 0.36 to 0.40 μm of $Si0_2$. The two BSOI suppliers use somewhat different approaches to thin the Si in the active layer. One BSOI supplier (supplier A) uses a hydrogen implantation and blistering process to cleave the device Si wafer at the range of the hydrogen implant. After the cleave, the Si is polished to the final desired thickness and to smooth the surface. The second BSOI supplier (supplier B) uses a plasma thinning tool to uniformly remove Si from a bonded pair that has been ground and polished to a few μm of Si over the buried oxide. Substrates were obtained over a period of time to give us insight into quality, reproducibility and overall improvements by the suppliers. Material parameters such as metal contamination, defects, and film uniformity have been routinely measured and are reported in this paper. In addition, device results such as threshold voltage control (Vt), mobility and subthreshold leakage will be compared for devices built on SIMOX or BSOI substrates. Data will also be reported on the effect of different materials on the transients in the drain current due to differences in generation lifetime. Finally, the gate oxide integrity for SOI will be compared to that of gate oxides grown on bulk Si. The data were obtained from several different lots processed in our line and therefore represent any variations that may occur in either the process or the material over time.

2. MATERIAL RESULTS

Top Silicon Thickness Uniformity - The impact of the top Si thickness uniformity on the threshold voltage, silicide process and the isolation module were reported previously.[1, 2] For the partially depleted devices we use in our 0.5 μm CMOS technology, we require a Si film thickness of 100 ± 10 nm under the gate oxide. This sets the acceptable limits on the variation in as-received Si uniformity. This limit has to consider all variations in the process flow prior to gate oxidation that will thin the Si, as well as any non-uniformities in the incoming SOI wafers from the suppliers. Recent improvements in SIMOX implanters have improved the uniformity such that this is not considered an issue for this technology.[2] As we have reported elsewhere, the uniformity across the BSOI wafers produced by supplier B is highly dependent upon the local thickness variations of the bonded pair prior to plasma thinning.[2] In this case, the across wafer range is 10 to 15 nm and is at the limit of acceptable uniformity. Recent BSOI wafers produced by the hydrogen blistering process have across wafer ranges comparable to SIMOX wafers but their wafer to wafer uniformity is not as tight since the final thickness is produced by a single wafer CMP rather than a batch implant.

Metal contamination - Prior to the early 1990's, SIMOX wafers suffered from metal contamination caused by ion beam sputtering of the beam line and end station. This problem was exacerbated relative to a nominal implant due to the extreme implant conditions associated with SIMOX production. This led to the coating of the beamline and other components of the beamline with Si to reduce any source of sputtered metal. The routine use of TXRF by SIMOX suppliers has resulted in a reduction of the metal surface contamination to levels that are consistently <1.0 x $10^{11}/cm^2$ for all metals.[2] This meets the specifications of

most current wafer fabrication lines. Comparable results have been seen on the BSOI wafers produced by supplier B. The BSOI wafers from supplier A have surface metal levels below the detection limit of TXRF. To further reduce the metal contamination and to understand the effects of metal gettering as a function of depth, more sensitive techniques such as ICPMS and AAS are being explored.[3]

Defects in the top silicon - Crystalline defects such as threading dislocation and stacking fault pyramids in the superficial Si layer and their formulation in SIMOX, have been studied in detail by Krause et al.[4] For standard dose SIMOX, we have observed dislocation densities that vary from ~3 x 10^{15} to ~2 x $10^{17}/cm^2$ depending upon the beam energy, current density and external substrate heating. These defects have always been a concern, but our device and gate oxide data have not shown them to correlate with device leakage or gate oxide breakdown.[5,6] However, there may be some correlation with the generation lifetime that is discussed in a subsequent section.[7]

A far more serious defect that we and others have found in the top Si layer is missing Si or pitting of the top Si surface.[2,8] The pits tend to be 0.1-0.5 μm in diameter. Although they are extremely difficult to detect in as-received wafers, these defects are easily detected by placing a wafer in concentrated HF acid for 10-15 minutes. The HF goes through the hole in the Si and etches the buried oxide, producing a void in the buried oxide that is ~25 μm in diameter and easily seen in an optical microscope. In many cases this pitting is associated with metal contamination. The metal forms a silicide that is etched out during the subsequent processing. Prior to the routine adoption of the HF test in 1994 this was a serious problem. Recently however, the density of HF defects has been less than $1/cm^2$ on both SIMOX and BSOI. The source of this lower level of defects remains to be understood and eliminated.

3. CMOS DEVICE RESULTS

We have used standard bulk Si process equipment and process modules to build CMOS devices, capacitors and circuits at the 0.5 μm design level. A simple LOCOS like isolation module was used in combination with a Ti salicide process. The devices are built with 100 nm of Si beneath a 10.5 nm gate oxide. A variety of MOS device parameters have been examined on different substrates and on several different lots. As seen in Fig. 1, we do not see any differences in Vt, mobility, etc. for the different substrates in a given lot.

Fig. 2 shows the typical lot to lot variation in Vt for SIMOX substrates for a given supplier and a given baseline flow. The within lot range is ~75 mV and 50 % of the devices tested are ±10 mV of the average. Also note that the lot to lot averages vary less than 50 mV showing that both the material and process can be quite reproducible.

The one device parameter that we do see major differences in substrate type is the generation lifetime. This can affect the transient effect in these floating body devices. The analysis technique has been reported by Shin et. al.[7] The lifetime for the different substrates is presented in Fig. 3. The lifetime is longest for the BSOI wafers from supplier B and shortest for the SIMOX wafers independent of supplier. The across wafer lifetime is ±.1 μS. The cause for the differences in lifetime is under further investigation.

4. GATE OXIDE INTEGRITY

The gate oxide breakdown voltage (BV) histograms for small ($2X10^{-5}cm^2$) capacitors on bulk Si, SIMOX and BSOI are identical.[2] (These capacitors are made as part of the process flow so that they are representative of the gate oxide on an MOS device.) When these results are combined with Fowler-Nordheim current-voltage measurements, and charge to breakdown measurements on similar capacitors, results indicate there are no intrinsic differences in the gate oxide quality. However, as reported by Hong et. al.[6] and shown here in Fig. 4, on large capacitors there is clear difference between capacitors on SOI and bulk Si. We very seldom see a breakdown on any material type that is less than 6 volts. However, the capacitors on SOI have a larger spread in the BV and show some early conduction independent of whether they are on SIMOX or BSOI. It should be noted that the SIMOX capacitors capture more than 1000 dislocations and this has no apparent effect on gate oxide BV. These results indicate that there is an area or process dependent issue that is specific to SOI.

Fig. 5 shows the effect of the pitting defects, that were discussed above, on the gate oxide capacitors. The defect density is ~$1000/cm^2$ and each capacitor captures ~3 defects. Since all capacitors on this material have BV less than 5V, these are truly killer defects and must be eliminated to build ULSI circuits with large gate area.

5. SUMMARY

For more than 3 years we have purchased BSOI and SIMOX wafers from commercial suppliers. These substrates have been evaluated for such material properties as uniformity, defects, metal contamination, etc. In addition, we have built MOS capacitors and devices using a 0.5 μm CMOS flow. We have seen very few differences between substrates and the properties of devices built on each type of substrate improves with optimization of the process flow. This implies that at least for the devices we are building, the results are more sensitive to the process integration than to the particular type of SOI substrate. The one difference in substrates is in the generation lifetime where differences of a factor of 6-7 were seen.

6. REFERENCES

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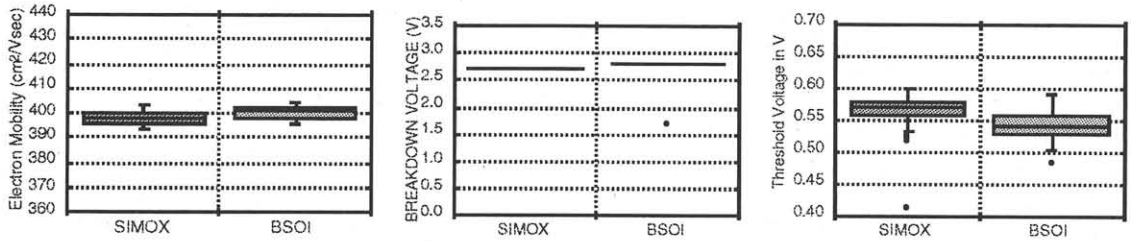

FIG. 1. Electron mobility, BVDSS and Vt for devices in a split lot of SIMOX and BSOI showing no significant difference with material type.

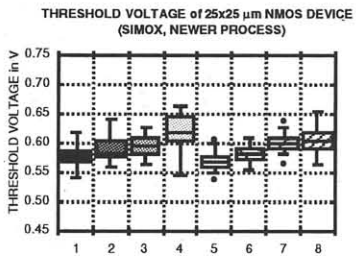

Fig. 2 Comparison of Vt on several lots of SIMOX wafers.

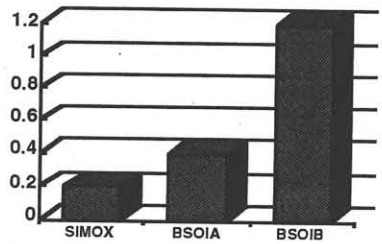

Fig. 3. Plot of generation lifetime in µSec for different SOI substrates.

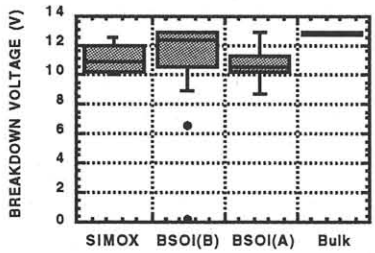

Fig.4 Capacitors showing the difference in BV for those on bulk and on SOI.

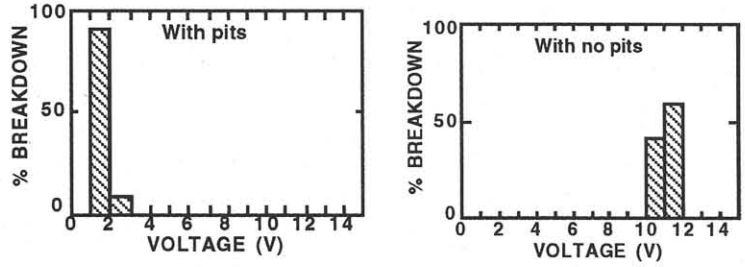

Figure 5. Comparison of gate oxide breakdowns for 3.6 X 10^{-3} cm^2 capacitors built on SIMOX with a high level of pitting defects and SIMOX wafers with a low level of pitting defects.