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Invited

Advanced SOI Devices Using CMP and Wafer Bonding

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This article is about the SOI (silicon on insulator) devices in which gate electrodes and capacitors are buried underneath a Si layer. We succeeded in developing a Double-gate CMOSFET and a SOI-DRAM chip using conventional CMP(chemical mechanical polishing) and low-temperature wafer bonding technology. These devices have excellent characteristics and are usually difficult to develop with conventional SOI wafers and Si wafers.

1. INTRODUCTION

There are two methods for fabricating SOI devices. One involves the use of SOI wafers from the very beginning of the fabrication process while the other involves the employment of SOI technology halfway through an LSI process. For the first method, which is most commonly used, both SIMOX wafers and bonded SOI wafers are required. The crystallinity of SIMOX wafers has also been greatly improved. Nevertheless, it has not reached the same level as the level of bulk wafers. Uniformity in the thickness of Si layer in bonded SOI wafers has been improved drastically using ELTRAN[1], PACE[2], and SMART-CUT[3], but there has not been any actual experience on a mass production scale. With the second SOI device fabrication method, on the other hand, variation in wafer quality can be avoided because SOI technology is applied halfway in the LSI process. The crystallinity of wafers produced using this method is stable and of high quality, regardless of the production scale and wafer size, because the wafers used are bulk wafers. Moreover, bonding substrates that already contain electrodes enables the incorporation of electrodes in an oxide film underneath a Si layer.

This article describes a inverted device SOI structure which is the second SOI device.

2. INVERTED DEVICE SOI STRUCTURE

There are three different types of devices that can be converted to SOI devices with an SOI structure implemented during a conventional LSI process as shown in Figure 1.

For the processing of type (A), the SOI structure is introduced after a field oxide film is formed. With this process, it is easy to planarize the wafer surface because initially, its surface is relatively smooth. Moreover, like the conventional bonded SOI wafers, type (A) can be bonded at high temperature. Therefore, it is easy to achieve a uniform bonding with the type (A) process[4),5)].

In the fabrication of type (B) devices, an SOI structure is created after the transistors are in place. In this case, the wafer surface is rough and difficult to polish. In addition, it is impossible to bond the wafers at high temperature because transistors have already been formed on the wafers[6)].

In the fabrication of type (C) devices, SOI structure is created after interconnection has been completed. In this process, it is more difficult to planarize the surface compared to the other processes. Moreover, it is necessary to decrease the bonding temperature to a great extent because the interconnection is already in place. For this reason, processing of type (C) usually requires that the wafers be bonded with adhesive[7)].

To achieve voidless bonding, it is necessary to polish the bonding surface to a flatness comparable to the surface of a thermally oxidized film. Another important challenge is to eliminate pattern displacement that may occur after the bonding and thin-film processes. When a pattern is displaced from its correct position, it becomes impossible to carry out lithography later.

3. FABRICATION TECHNOLOGY

3-1. Planarization using CMP

The CMP process is being used to process many products and has been recognized as a typical LSI processing technique. The existing CMP process is capable of this requirement and there is no need to develop a new process.

If transistors have been formed on the substrate, step height on the surface can be as large as 500 nm or more. We achieved a desired flatness using hard pad (IC1000 single) instead of the stacked pad. Figure 2 shows the flatness achieved using stacked pad and head pad. Use of hard pad reduced the residual step height to 1/10 of the level achieved with stacked pad. As shown in the figure, by using hard pad, the flatness required for low-temperature bonding can be easily obtained with only a small amount of polishing. The typical CMP technique produces much of the same result with bulk surfaces of surface roughness, surface particles and surface contamination.

3-2. Low-temperature bonding technology

When substrates with previously formed transistors are bonded, the applicable annealing temperature is lower. To meet this requirement, substrate surfaces are coated with low-melting glass a BPSG film, and planarized using CMP. Figure 3 shows the bonding strength of various bonding configurations. The bonding strength between a BPSG film and oxide film bonded at 800℃ for 10 minutes is comparable to that between an oxide film and Si bonded at high temperature[8)]. The bonding temperature and time do not influence the diffusion profiles of impurities in transistors.

3-3. Producing a thin Si layer by selective polishing

With Selective polishing, where a field oxide film is used

as the polishing stopper, a uniform thin film can be obtained by CMP without being affected so much by the TTV(total thickness variation) of the base wafer. With this technique, the in-plane uniformity can be improved; however, dishing may occur if the gap for the polishing stopper is large. To improve the thickness uniformity of a Si layer, one effective way is to deposit an etching proof layer prior to the formation of the Si layer, and use selective etching to replace the polishing process. Figure 4 shows thickness variation in a Si layer formed on a p on p^+ epitaxial wafer by selective etching. Variation in the thickness of the Si layer was reduced to the same level as that of an epitaxial Si layer. The amount of polishing required for the Si layer after selective etching was less than 0.7 μm, and the TTV effect was insignificant. Dishing can almost be completely eliminated by using a CMP monitor to determine the end point for selective polishing eliminating excessive polishing[9].

3-4. Pattern displacement

The pattern displacement varies with the bonding temperature, oxide film type, and bonding method. Figure 5 demonstrates how far a pattern can be displaced from its designated position during the polishing process. When wafers with nondoped CVD oxide films are bonded at the usual 1100 ℃ , the pattern displacement increases. Meanwhile, the displacement significantly lessen for low temperature bonding with a BPSG film. Figure 6 shows the pattern displacement profile resulting from a high temperature heat treatment performed after pre-bonding substrate pressed at the center. The pattern displacement around the center demonstrates that stress applied before bonding cannot be removed even when a high temperature heat treatment is applied. For this reason, we used a BPSG film on the device inversing SOI structure for bonding the wafers at low temperature after pre-bonding without applying any central pressure. In this case, no aggravation in displacement was observed after the polishing process.

4. APPLICATIONS

4-1. Double-gate MOSFET[10),11)]

A MOSFET with gate electrodes both over and underneath the channel was proposed and named XMOS by Sekigawa et al. in 1984.[12)] Simulation has demonstrated that this Double-gate structure can be used to accommodate a gate length of up to 0.035 μm because the short channel effect can be greatly suppressed with this structure[13)].

Figure 7 shows the process flow. We optimized Vth by fabricating the front and the back gates using p^+ polysilicon and n^+ polysilicon, respectively. The Vth of transistors with an SOI film thickness of 40 nm is 0.17 V (nMOS) and -0.24 V (pMOS). The delay time in a 0.19 μm ring oscillator is 27 ps (for V_{dd} of 2 V), and the power consumption is 1/3 of that of a bulk MOSFET (with a channel length of 0.15 μm) of the same speed.

4-2. SOI-DRAM

With the SOI structure, lower cell capacitance, and hence smaller size capacitors leading to small-size chips become feasible due to the reduction of soft error. Nishihara et al. have developed a DRAM chip in which capacitor cells are buried in an oxide film with the word lines and the bits lines on the surface[6)].

We have proposed a Reversed-STacked-Capacitor (RSTC) cell with an SOI substrate containing not only cells but also word lines and source/drain diffusion layers[14)]. Figure 8 is a picture of the cross-section of the RSTC-cell. Figure 9 shows the SEM image of the cross section of a portion where the word lines and 64-Mbit fin capacitors were. The SOI film was 97 nm +/-8 nm in thickness and free of voids. With the DRAM wafer, the bit-line capacitance was reduced to half of that with a conventional shielded bit line DRAM chip. The bit- capacitance to the cell plate and to the word-lines were reduced to 1/3 and 2/3, respectively.

5. SUMMARY

The SOI device, being fabricated from a bulk wafer, requires no conventional SOI wafers. CMP machines and technologies originally developed for multilayer interconnection can be used to fabricate SOI structures from bulk LSI wafers. Furthermore, this SOI structure enables the forming of various electrodes in an oxide film underneath the Si layer. The device inversing SOI structure is expected to be applied in various LSI chips and eventually promote the development of new Si devices.

6. ACKNOWLEDGMENT

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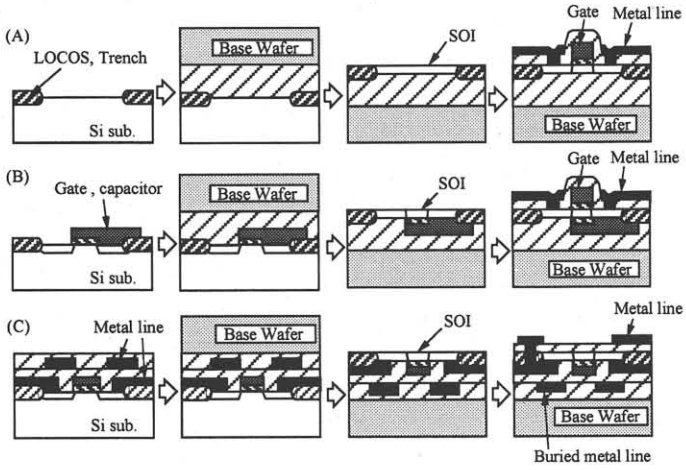


Figure 1. Inverted-device SOI Sutructure

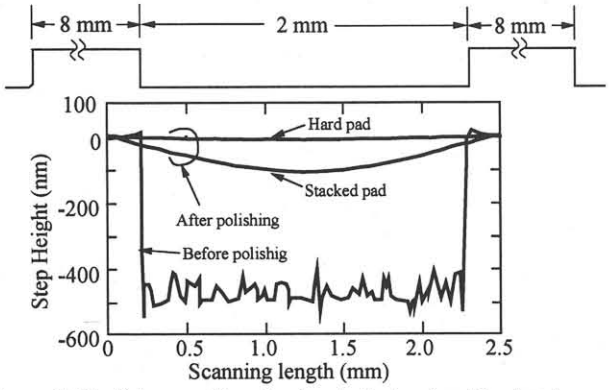


Figure 2. The flatness achieved using stacked pad and hard pad
Stacked pad : IC1000/Suba400
Hard pad : IC1000

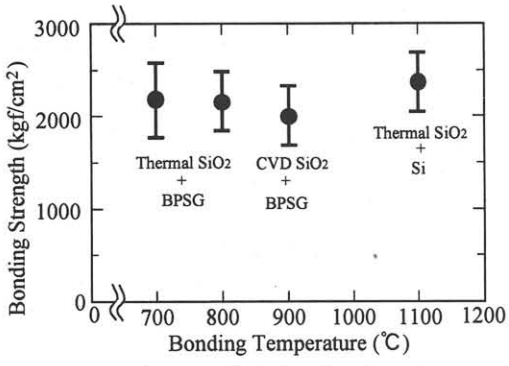
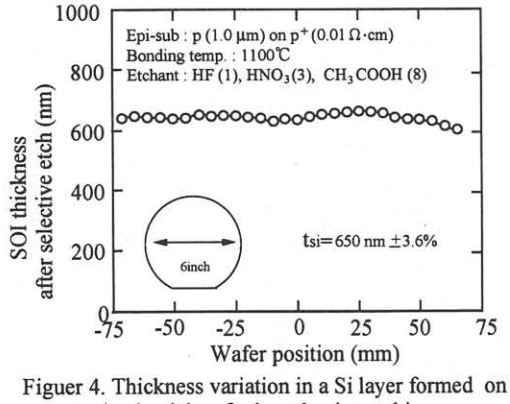


Figure 3. Wafer bonding strength



Figuer 4. Thickness variation in a Si layer formed on a p on p^+ epitaxial wafer by selective etching.

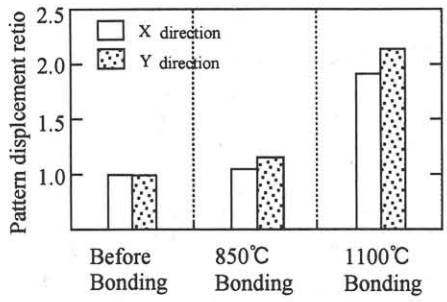


Figure 5. Pattern displacement of inverted SOI wafer

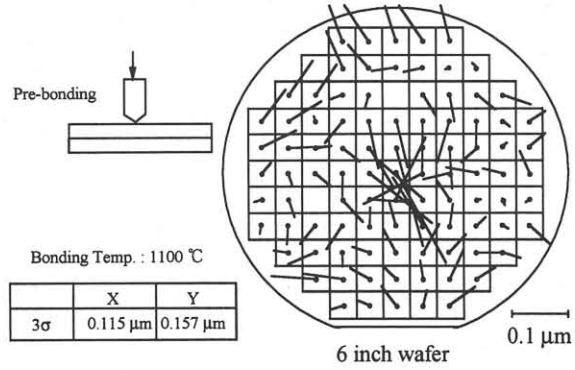


Figure 6. Pattern displacement profile

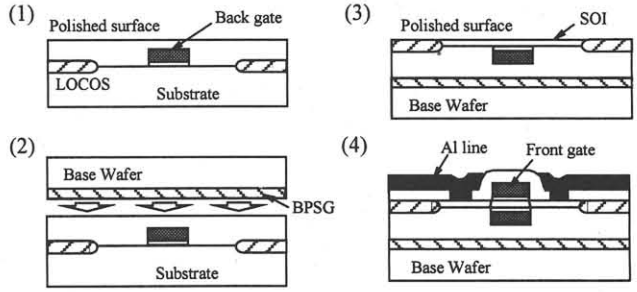


Figure 7. Double -gate Process sequence

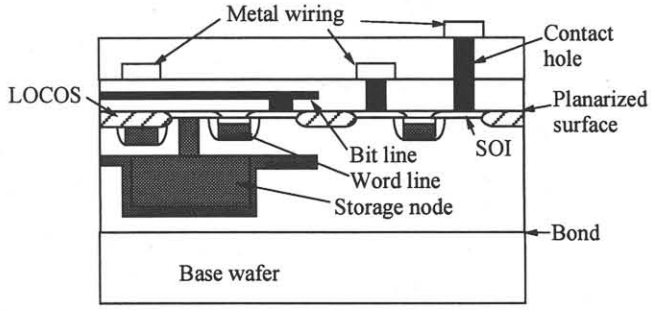


Figure 8. Cross sectional of RSTC cell DRAM

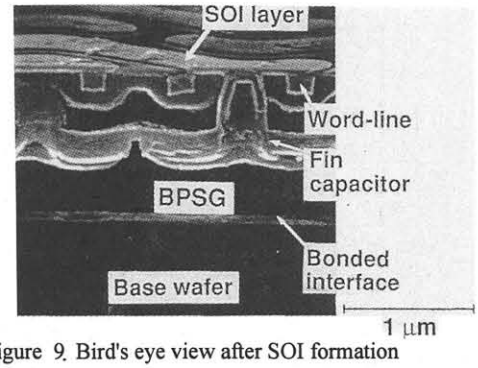


Figure 9. Bird's eye view after SOI formation