Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 482-484

Invited

LSI Applications of 0.25-μm CMOS/SIMOX Technology

Masayuki INO, Toshiaki TSUCHIYA, Ken TAKEYA and Tetsushi SAKAI*
*NTT LSI Laboratories, * NTT Electronics Technologies Ltd*
3-1, Morinosato Wakamiya, Atsugi, Kanagawa 243-01, Japan

Various circuits were fabricated using fully-depleted 0.25-um gate MOSFETs on a low-dose SIMOX substrate. The operating speeds of the I/O circuits and MUX/DMUX circuits were higher than 2.4-GHz. A 300-KG (3-M transistors) gate array LSI was also fabricated. The performance of a 120-KG test LSI was compared to that of a bulk/CMOS gate array. The operating speed of the 0.25-um SIMOX LSI was 10% higher than a 0.25-um bulk LSI with 35% less power. The power dissipation of the LSI can be reduced to 1/40 that of the 0.5-um LSI at the same speed.

1. INTRODUCTION

Silicon-on-insulator (SOI) devices have several advantages for high-speed, low-power, and low-voltage LSIs, such as small parasitic capacitances. But there were some problems in using them for CMOS LSI applications. Among them, the quality of the substrate and the floating body effect are significant problem, but these have been solved by a low-dose high-quality SIMOX substrate and fully-depleted device development in the deep sub-micrometer region. In this paper, we describe SSI and LSI fabrication results using 0.25-um CMOS/SIMOX. We fabricated a 0.25-um CMOS/SIMOX 300-KG gate array LSI with a VDD of 2 V, adopting a new interface circuit that is compatible with 3.3 V CMOS or LVTTL and has a high ESD hardness with above 2000 V.

2. DEVICE FABRICATION PROCESS

We adopted a low-dose, high-quality, 6-inch SIMOX wafer[1] with an oxygen dose of $3\text{-}5\times10^{17}cm^{-2}$, and annealed it at 1350 ℃. This was followed by oxidation at the same temperature. The newly developed SIMOX wafers have high uniformity in the top silicon layer and buried oxide thickness. The top silicon layer is nearly defect free at less than 300 cm^{-2}.

Fully-depleted (FD) devices fabricated on the SOI structure have additional advantages such as the no-kink property, sharp threshold slope, and reduced short-channel effects. FD devices are almost free from floating body effects, although partially-depleted devices need body contact to suppress these effects. FD devices have been found to be dynamically stable[2], even without body contact. This is another advantage of FD devices and allows high density layout and LSI design compatibility with bulk devices.

We fabricated various circuits, including SSIs, such as interface circuits and MUX/DMUX, as well as a 300-KG CMOS gate array LSI using a 0.25-um-gate SIMOX and bulk device technologies. Fully-depleted dual-gate type n and p MOSFETs with 5-nm-thick gate oxides were made on 50-nm-thick SIMOX films. We developed a new technology involving Ar ion implantation into S/D regions[3], which effectively suppresses the parasitic bipolar action. Figure 1 shows a cross-section of CMOS/SIMOX devices. The key features of the 0.25-um device and interconnection technologies are summarized in Table 1. Supply voltages (VDD) are 2 V for SIMOX and 2.5 V for bulk. We fabricated various circuits using these two kinds of devices to compare performance. The designed threshold voltages of the SIMOX can be set lower at the same standby current level because these devices have a steeper subthreshold slope than the bulk devices. The perfect planarization technique enables a fine pitch of 1.4-um (via to via) for all four metal layers and stacked vias/contacts. KrF excimer laser lithography was used for all layers.

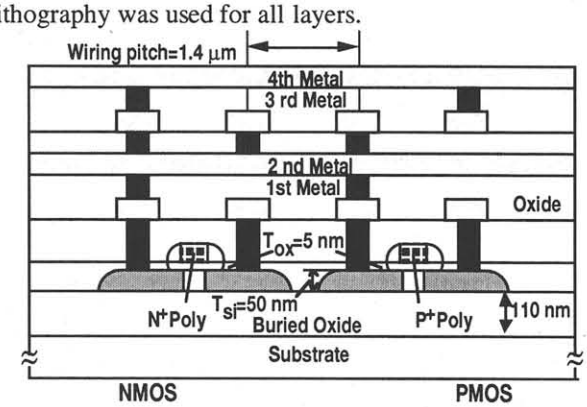


Fig.1 Cross-section of CMOS/SIMOX device.

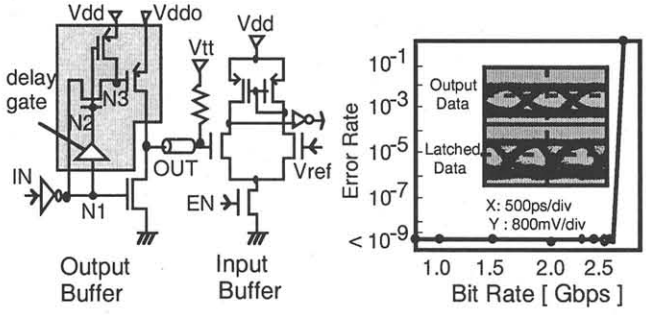
Table 1 Features of 0.25-um device and interconnect.

	SIMOX	BULK
VDD(V)	2.0	2.5
	NMOS / PMOS	NMOS / PMOS
Lg (μm)	0.25 / 0.25	0.25 / 0.31
Tox (nm)	5	6.5
T_{Si} / T_{BOX} (nm)	50 / 110	-----
Gate poly-Si	N^+ / P^+	N^+ / N^+
Vth(V)	0.2 / -0.3	0.3 / -0.4
Metal-Pitches	1.4μm for AL1, AL2, AL3, AL4	
Via	stacked Via / Contact (0.36μm□)	

3. SSI APPLICATIONS

High-speed and low-power I/O and MUX/DMUX circuits have been required as key components in high-speed digital systems such as ATM switches and optical communication systems.

We developed a new low-voltage-swing, GHz interface circuit, the active-pull-up (APU) circuit.[4] Figure 2 shows the circuits configuration and the measured performance of the APU interface circuit fabricated using 0.25-um CMOS/SIMOX. Owing to the the active-pull-up, the APU is 1.4 times faster than the conventional open-drain type circuit (GTL). The maximum operating frequency of the 0.25-um SIMOX is 2.6-GHz, which is 1.5 higher than that of 0.25-um bulk.



(a) APU interface circuit (b) 2.6Gb/s eye pattern

Fig.2 APU interface circuit and 2.6 Gb/s eye pattern.

MUX and DMUX circuits were fabricated using 0.25-um technology. We adopted the 2:1 selector-type architecture, in which an average fanout count is small at 1.1 for the MUX circuit.[5] We chose this because in a SIMOX device, the junction capacitance is small but the gate capacitance is almost the same as that of a bulk device. The operating frequencies and power consumptions of the MUX circuits are shown in Fig. 3. The maximum frequency of the SIMOX circuits was 2.7-GHz for the MUX and over 3 GHz for the DMUX. These values are 25% higher than those of the bulk. These results show that a 2.4 Gb/s interface, equivalent to four times 622 Mb/s can be made with 0.25-um CMOS/SIMOX and that this is useful in communications applications.

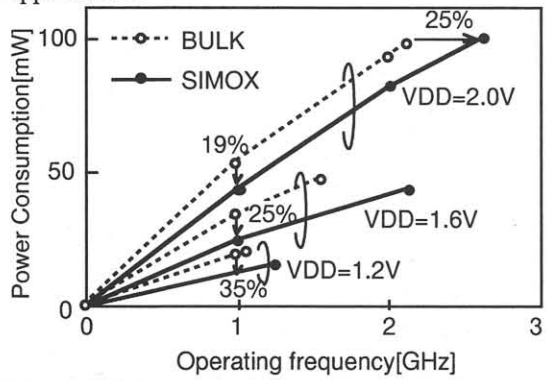


Fig.3 MUX power dissipation vs. operating frequency.

4. GATE ARRAY LSI APPLICATIONS

Figure 4 shows a microphotograph of a fabricated SOG-type gate array LSI[6] with a 10-mm square chip size, which consists of about 300 K basic cells (3-million transistors). One basic cell contains ten transistors and a two-port sRAM cell can be constructed using one basic cell. The same layout pattern was used for SIMOX and the bulk LSIs, because this made it easy to compare performance. We fabricated a test LSI with a 120-KG and 8.7-Kb two-port memory on the gate array. This LSI function was achieved using a 0.5-um CMOS gate array for a switching system. As a result, LSI performance can be compared for the 0.5-um bulk CMOS, 0.25-um CMOS/SIMOX, and the 0.25-um bulk CMOSs.

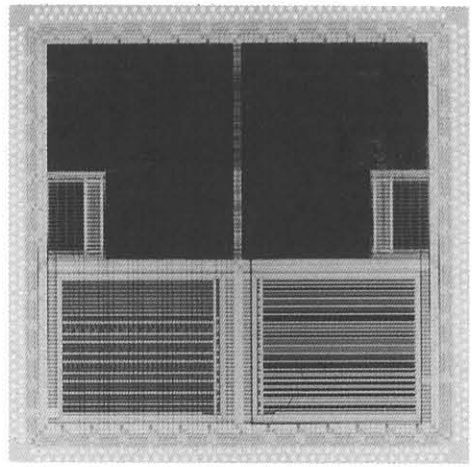


Fig.4 Microphotograph of a 0.25-um gate array LSI.

The tpd of the inverter (F.O= 1) is 50 ps, the loaded delay time of a 2-input NAND when F.O= 3 and AL=1-mm is 190 ps for a normal gate and 110 ps for a power gate in the 0.25-um SIMOX gate array. These are 15 to 20% faster with 45% less power than those of the 0.25-um bulk. Typical access times of a 13-kb sRAM macro on the gate array are 3.5 ns for SIMOX and 4 ns for bulk.

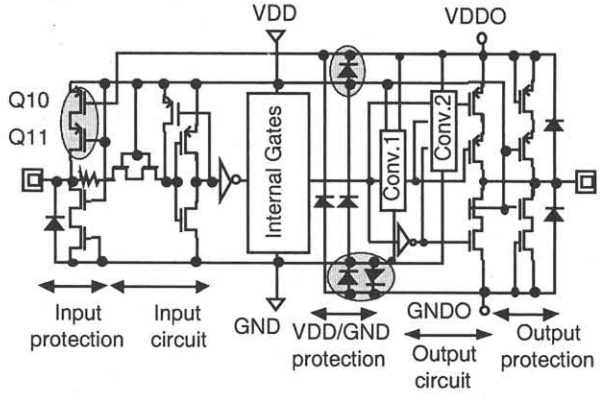


Fig.5 I/O circuit for gate array, with ESD protection.

The key technology for broader use of SOI LSI is an interface circuit that is compatible with a supply voltage of 3.3 V and is highly tolerant for ESD. We developed an interface circuit[7] compatible with 3.3 V CMOS and LVTTL with an over 2000 V ESD-protection circuit for a 0.25-um gate array, as shown in Fig.5.

Fully-functional operation for two kinds of LSIs using 0.25-um gate devices were confirmed by the measurements. The fault coverage of the LSI was over 95% because of the use of scan technology. The measured speed-power of the LSI is shown in Fig.6 The maximum operating frequency of the 0.5-um LSI was 30 MHz, with a power dissipation of 1300-mW at VDD = 3.3 V. The maximum frequency of the

0.25-um SIMOX was 76 MHz, with 315-mW power dissipation at VDD = 2 V. Therefore, using 0.25-um SIMOX, the speed is 2.5 times higher with 1/4 lower power dissipation compared to 0.5-um bulk. For the 0.25-um bulk, at VDD = 2.5 V the maximum speed is 70 MHz which is 10% lower than the SIMOX with 35% larger power dissipation at 490 mW. The supply voltage of the SIMOX can be lowered at 1.2 V to attain the same speed as the 0.5-um bulk, reducing power dissipation to about 1/40 (34/1300).

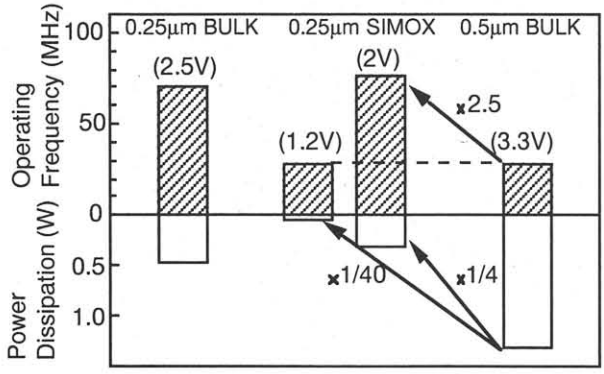


Fig.6 Speed-power comparison of gate array LSIs.

5. DISCUSSION

Figure 7 shows VDD dependencies of the loaded gate delay times (2NAND, F.O=3, Al=1 mm), the cycle times of the test LSIs, and the S/D junction capacitances (Cj) for SIMOX and bulk devices. The speed dendence of the LSI on VDD almost agrees with that of the loaded NAND gates. As the supply voltage was decreased, this speed difference between SIMOX and bulk widened as shown in Fig.7, and at VDD = 1.2 V, the bulk LSIs could no longer operates, while the SIMOX LSI still operated perfectly. This tendency is explained by Cj dependence on VDD and the lower threshold voltage in SIMOX than in bulk considering the same standby current level.

Average critical path load capacitances of the test LSI on the gate array and the MUX are shown in Fig.8, both for bulk and SIMOX circuits. In SSI such as the MUX, wiring capacitance is small and the load capacitance is determined by the device capacitances. Therefore, S/D capacitance reduction in SIMOX is effective in reducing total load capacitance. This is the main reason for higher-speed operation in SSI such as I/O circuits, frequency dividers, MUX/DMUX using SIMOX compared to those using bulk. Especially in this MUX circuit, since fanout loads (gate capacitances) were minimized in the design, the total capacitance of the SIMOX can be reduced to 61.7% of the bulk. On the other hand, the wiring capacitance becomes large at about 70% of total capacitances in the LSI. The shares of the each capacitance in the wiring capacitance are 45% for line to substrate, 30% for neighboring line, and 25% for inter layer. Only the line to substrate capacitance can be reduced in SIMOX, and the other two kinds of wiring capacitances are almost equal to those in bulk. Using SIMOX, the total load capacitance improvement was relatively small (10.7%) in the LSI in which the same layout design was employed for both bulk and SIMOX. This value almost coincides with the LSI speed improvement. Speed performance of SIMOX LSI can be improved by design optimization and interconnect technology advances such as using a low permittivity or thicker interlayer insulator.

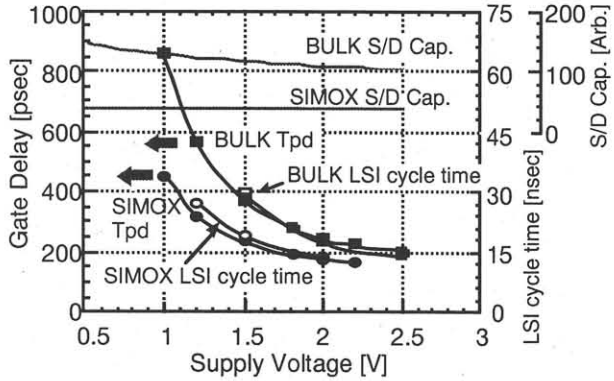


Fig.7 VDD dependencies of tpd, LSI speed, and Cj.

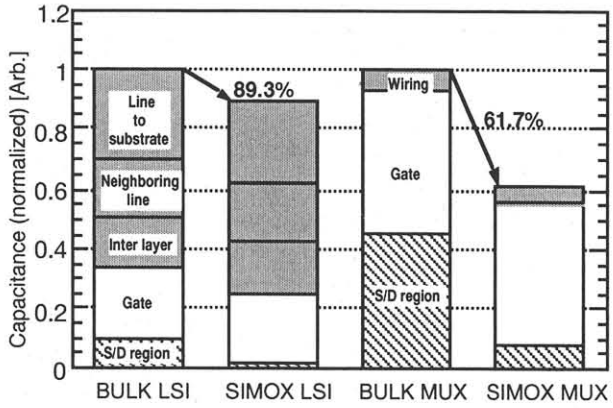


Fig.8 Load capacitances in the LSI and MUX.

6. CONCLUSION

A 0.25-um gate CMOS/SIMOX LSI and variable SSIs weres realized by adopting fully-depleted devices on a low-dose SIMOX, and their performance advantages were confirmed. From the I/O and MUX/DMUX fabrication results, a 2.4-Gb/s interface which is useful in communications applications, can be made using 0.25-um SIMOX. Results of 120 KG test LSI on a gate array shows that power dissipation of the 0.25-um SIMOX LSI can be reduced to 1/40 that of the 0.5-um LSI at the same speed.

REFERENCES

1) S.Nakashima, J. Mater.Res. **8** (1993) 523
2) T.Tsuchiya, Proc. SOI Conf. (1994) 401
3) T.Ohno, Tech. Dig. IEDM (1995) 627
4) Y.Ohtomo, Trans. IEICE, **E79-C** (1996) 524
5) S.Yasuda, Trans. IEICE, **E78-C** (1995) 1746
6) M.Ino, Tech. Dig. ISSCC, **TP 5.5** (1996) 86
7) Y.Ohtomo, Proc. CICC, **4-3** (1996) 57