

Invited

Dielectric/Silicon Interface Structures and Electrical Properties

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Electrical properties of ultrathin dielectric films on silicon depend on physical properties of an interfacial layer between the dielectric and silicon. The interfacial layer is a structural transition layer and/or a compositional transition layer, which has different properties from the bulk. The present work shows three examples of the interfacial layers such as SiO₂/Si, Si₃N₄/Si, and Ta₂O₅/Si. Device process technology is responsible for engineering the structural and/or compositional transition layer in order to realize gigabit era.

1. INTRODUCTION

With downscaling of dielectric film thickness in ultra-large scale integrated (ULSI) devices, there are new concerns on electrical properties of ultrathin dielectric films. The thickness range is less than 10 nm in SiO₂ equivalent thickness. Those ultrathin dielectric films have degraded electrical properties compared to what the bulk films predict. It is caused from the interfacial layer which is a structural transition layer and/or a compositional transition layer. The interfacial layer between dielectric and silicon is inevitably formed due to growth mechanism of the dielectric films. Targets of device process technology is to find how to minimize the interfacial layer formation and how to improve its electrical properties.

2. SiO₂/Si

Although there are many reports on SiO₂/Si interface structures, the conclusions are a little bit confused. For instance, XPS studies produce both a compositional transition layer and a structural transition layer. Backscattering spectroscopy measurements conclude that an SiO₂ film is stoichiometric to approximately one monolayer at the interface. The transition layer thickness is also confused. According to lattice image TEM observations, the transition layer thickness is a few atomic layers. But the thickness obtained by XPS and etching speed studies is reported to be several nanometers, which is suitable for explaining electrical properties.

The present work shows that a 7-8 nm thick structural transition layer of SiO₂ is formed at the SiO₂/Si interface by thermal oxidation of Si [1]. The transition layer density is measured using grazing-incidence diffraction of synchrotron radiation, and found to be around 2.4 g/cm³ which is larger than bulk SiO₂ density (2.2 g/cm³). When Fowler-Nordheim tunneling current is injected into a thin SiO₂ film, the dielectric breakdown mainly occurs in the structural transition layer because of Si-Si bond formations due to hypervalent properties of Si atoms and compressive stress. Introduction of nitrogen atoms into the transition layer improves injected charge-to-breakdown of the thin SiO₂ film due to stress relaxation. The structural transition layer seems to be formed by volume expansion due to thermal oxidation of Si, because the transition layer is not observed in CVD oxides. Two-layer model for SiO₂ film structure has been already proposed by Tiller in 1983. Recently, in addition to the present work, some FT-IR and neutron analysis studies support the two-layer model.

E' center is considered to behave as a hole trap, and its origin is said to be an oxygen deficiency. But a vacancy of a negatively charged atom becomes usually an electron trap as seen in ionic crystals and II-VI compound semiconductors. Some theoretical studies about E' center have been reported, and

suggested that E' center is both an electron trap and a hole trap, and that a hole trap is more probable. However, those studies are based on semi-empirical molecular orbital (MO) calculations, which can not obtain the accurate total energy. To make it clear which traps (i.e., electron traps or hole traps) are more probable in SiO₂, ab initio MO calculations are carried out in the present work. The electron affinities of an oxygen vacancy site is positive. Namely the extra electron can be trapped around the oxygen deficiency site. Because of the strong electronegativity of oxygen atoms, Si atoms become positively charged in SiO₂. Thus, the oxygen deficiency site is a proper place to accept the extra electron, since the lack of the oxygen atom reduces the electron repulsions in that area. This seems to be the reason why the oxygen deficiency site has the positive electron affinity. The positive electron affinity is obtained by the SDCI+Q calculation after the Hartree-Fock (HF) calculation. This negative correlation energy is called "negative U" in computational physics, and the negative U defects are attributed to a vacancy in Si single crystal and a nitrogen deficiency site in Si₃N₄. Therefore, it is reasonably concluded that an oxygen deficiency site is an electron trap in SiO₂. E' center seems to be a structural defect deformed from an oxygen deficiency site, and to behave both an hole trap and an electron trap.

3. Si₃N₄/Si

In a chemical vapor deposition (CVD) reactor, an SiH₄ and NH₃ gas mixture produces silylenes (X-Si-Y; X and Y are substituents). Insertion of silylene into Si-H and N-H bonds on an Si₃N₄ surface is the important part of the CVD film growth mechanism. Following the insertion, H₂-elimination reaction occurs from the surface. To obtain the reaction energies of these insertion and H₂-elimination reactions, ab initio MO calculations are carried out [2].

The experimental observations, that many Si-H and N-H bonds are contained in an SiN_x CVD film, support the H-terminated surface model. This is because Si-H and N-H bonds seem to result from missing the insertion and H₂-elimination reactions of these bonds during the growth. The CVD film growth mechanism proposed here also explains that an SiN_x film composition deposited by using SiH₄ and NH₃ is Si-rich. According to the mechanism, Si atoms are incorporated by SiH₂ and SiNH₃ insertion reactions into surface Si-H and N-H bonds, while N atoms are incorporated only by SiNH₃ insertion reactions. Therefore, the film composition is inevitably Si-rich. Consequently, in a conventional SiN_x CVD reactor, NH₃ flow rate has to be much higher than SiH₄ flow rate to minimize the compositional deviation from the stoichiometry.

To improve ultrathin SiN_x film quality for a stacked capacitor, we can obtain a prediction from the model for the SiN_x CVD film growth mechanism. Namely a transition layer exists in the SiN_x film which is deposited on native oxide of silicon. Since there is no surface Si-H and N-H bonds on the native oxide, heterogeneous three dimensional nucleation of silicon must happen before the subsequent SiN_x film growth. Therefore, there seems to exist an Si-rich transition layer between the native oxide and the bulk SiN_x film. The electrical properties of stacked capacitor will be much improved, if we can prepare an SiN_x film without the transition layer.

Therefore, an SiN_x film is suggested to be prepared using rapid thermal nitridation (RTN) prior to LPCVD. Based on secondary ion mass spectroscopy and x-ray photoelectron spectroscopy measurements, a stoichiometric SiN_x layer is formed in the case of RTN. On the contrary a conventional LPCVD SiN_x film on native oxide of silicon shows large Si 2p chemical shifts and high oxygen concentration around the nitride/silicon interface. In RTN+LPCVD method, an LPCVD SiN_x film on an RTN film increases the total film thickness without the transition layer formation, and shows much lower leakage current characteristics than an conventional LPCVD SiN_x film.

3. Ta₂O₅/Si

A Ta₂O₅ capacitor with a permittivity value of around 25 has a merit that they can be replaced an Si₃N₄ capacitor without major DRAM device structure. Ta₂O₅ films are usually prepared by LPCVD

using a Ta(OC₂H₅) and O₂ gas mixture. After the deposition, the film is annealed to suppress leakage current due to oxygen deficiency and included hydrocarbons. However, the annealing in oxygen atmosphere oxidizes storage node polysilicon, because oxygen molecules easily reach the polysilicon through a Ta₂O₅ film. Accordingly the effective permittivity value becomes less than 25. It is needed to prevent this oxidation of the storage node polysilicon to form ultrathin Ta₂O₅ capacitors with high permittivity [3].

RTN treatment was introduced to suppress oxidation of the storage node polysilicon during the annealing in oxygen atmosphere. RTN treatment was carried out at temperatures ranging from 800-1000C for 60 seconds in NH₃ under atmospheric pressure, just after cleaning the storage node polysilicon surface with diluted HF. The oxygen, nitrogen, and silicon depth distribution profiles of Ta₂O₅ capacitors were analyzed using SIMS. The nitrogen signal is detected at the interface between the Ta₂O₅ film and polysilicon with RTN, but is not detected for the sample without RTN. The oxygen signals at the interfaces of as-deposited samples are clearly different between RTN and no-RTN, and much lower in the case of the RTN treatment. These results indicate that the oxidation of storage node polysilicon leads to the formation of an SiON or SiO₂ layer.

Figure 1 shows a cross sectional TEM photograph for a Ta₂O₅/SiON/Si structure corresponding to (dark area)/(amorphous image)/(lattice image). The top amorphous area is a glue layer. The interfacial SiON layer is about 2.5 nm thick, and corresponds to a 2.0 nm equivalent thickness because of the higher dielectric constant compared to SiO₂. The Ta₂O₅ film thickness is around 9.0 nm, and corresponds to the 0.5 nm SiO₂ equivalent thickness. Accordingly, the total equivalent thickness is 2.5 nm, which is thinner than that of the no-RTN sample. If it is possible to suppress the oxidation of storage node polysilicon completely, the equivalent thickness will reach the 1.5 nm equivalent thickness.

4. Summary

With decreasing dielectric film thickness in ULSI devices, electrical properties of the film are changed from bulk properties, and depend on the interfacial layer. In this talk, three dielectric/ silicon interface properties were introduced as the key issues of ULSI devices. There are other concerns on dielectric/metal, metal/metal, and metal/silicon interfaces such as high permittivity material/electrode and interconnection structures in gigabit era. Device process technology is responsible for engineering those interfaces.

References

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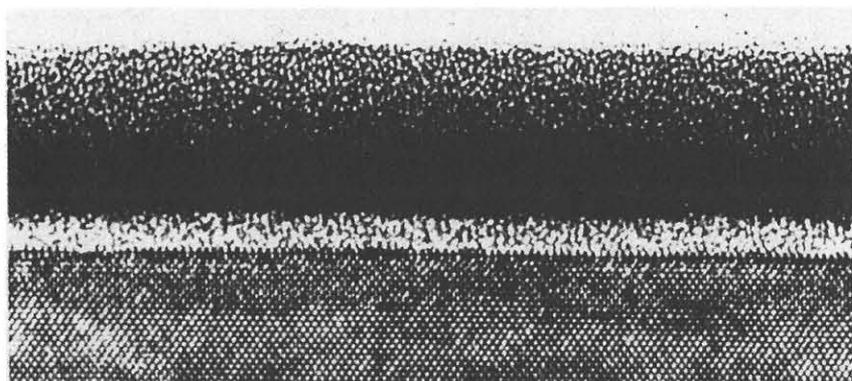


Fig 1. Cross sectional TEM image of Ta₂O₅/SiON/Si with RTN.