Invited

Dielectric Properties of Very Thin Films of Ba_{0.70}Sr_{0.30}TiO₃

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The drive to qualify high ε materials for advanced DRAMs has intensified in the past 3 years, and excellent progress has been made with BaSrTiO₃ (BST) films. Several issues will determine the usefulness of capacitors with thickness approaching 20 nm, including reliability. This paper describes leakage currents less than 10⁻⁷ A/cm² at ±1.1V for CVD BST films as thin as 8 nm, and resistance degradation studies indicate lifetime >10³ years at 1.6V for 24 nm films.

1. INTRODUCTION

At present there is a well recognized need for increased capacitance areal density in advanced DRAMs, i.e., for 256 Mb and future generations. Conventional silicon oxide and nitride dielectrics are the standard, and DRAM manufacturers are faced with greater and greater cell complexity in order to realize adequate capacitance. An alternative solution is to use more complicated dielectrics with higher relative permittivity (ϵ) enabling simplified capacitor geometry and associated fabrication processes. The predominant choice for the high ϵ dielectric has been (Ba,Sr)TiO₃ (BST) based on its dielectric properties, low leakage, and chemical stability.

2. EXPERIMENTAL

Several major steps towards the use of BST in advanced memories have been made over the past three years. Suitable dielectric and dc leakage properties have been demonstrated, viable integration schemes have been identified^{1,2,3} and no fundamental obstacles have been identified, although reliability and yield remain as key issues. At this time the foremost challenges involve realization of BST film properties on submicron structures and the development of manufacturing equipment, especially the BST CVD module and an electrode patterning tool.

Films described in this paper were deposited by CVD in a new tool developed by Varian. Precursors were delivered using the liquid delivery technique, and deposition conditions were reported previously.⁴ The deposition rate was 8 nm/minute. The Varian BST tool is capable of uniform deposition on both 150 mm and 200 mm wafers, and it is available as a manually loaded stand-alone module or as a cluster tool combined with a sputtering module. Thickness repeatability (run-to-run) is 2% (standard deviation) and composition repeatability is limited by measurement precision⁵ for 30 nm films, at approximately 0.35 atomic % (for the 50 atomic % target).

Long term stability of the tool is also very good for this stage in its development, and no drift in composition or thickness was observed after usage of precursor equivalent to 1,200 deposition runs for 30 nm BST thickness. This is particularly encouraging given the thermally labile nature of the Ba and Sr precursors used⁶, and this system of precursors and delivery technology⁷ remain the leading candidates for CVD of BST when a manufacturing process is adopted.

3. LEAKAGE CURRENTS FOR THIN BST FILMS

Continuing refinements in control of deposition conditions and electrode preparation have resulted in BST films less than 20 nm thick with leakage currents suitable for use in ULSI DRAMs. Figure 1 shows leakage current vs. thickness for Pt/BST/Pt capacitors at ±1.1V. Leakage was measured using an HP4145 Parameter Analyzer and I vs. V was scanned at 0.05 MV/cm every 5 sec. Measured leakage currents were less than 10⁻⁶ A/cm² for all BST thicknesses as low as 8 nm Except for the 12 nm samples, the + polarity leakage is nearly constant, while the negative polarity values are approximately one decade higher. This asymmetry can be attributed to differences in

current injection from the top electrode versus the bottom electrode BST interface.⁸ The detailed differences in properties of these two interfaces are not well understood.





4. CONTROL OF ε FOR THIN BST

For the sample set described above electrodes were made using e-beam evaporation through a shadow mask, which is useful for looking at basic material properties. Capacitance was measured using an HP 4192 LCR meter. Capacitance areal density of 71 fF/ μ m² was achieved for 24 nm BST thickness. The capacitance data was fit to a series capacitance This type of model allows one to model. examine whether the dielectric may be made up of some thin interfacial low dielectric constant layers at the electrode interfaces (inverse storage density = A/C interface ; total interface thickness = t_i), and a high dielectric constant film of thickness (t-t_i) with dielectric constant ε . This leads to the following equation for inverse storage density (A/C).9

$$A/C = A/C_{interface} + A/C_{bulk}$$

= A/C interface +
$$(t-t_i)/(88 \epsilon)$$
 (1)

Rearranging to show explicitly the slope and intercept:

$$A/C = \{A/C_{\text{interface}} - t_i / (88 \varepsilon) \} + t(1/88 \varepsilon)$$
(2)

Assuming the model is valid and the interfacial capacitance term is dominant, the bulk film dielectric constant and series capacitance can be calculated from the slope and intercept.¹⁰ The capacitance data fit the model well. For this

sample set, $(C/A)_{series}$ was found to be 147 fF/ μ m² and ϵ for the "bulk" part of the film was found to be 305. Electrode processing can have significant effects on thickness dependence of capacitance for thin films, and these influences are under investigation.

One possible explanation of the data is a low dielectric constant layer exists at the top electrode interface, although other physical mechanisms are possible and could give rise to a similar linear dependence of A/C on thickness. Given the absence of significant dispersion in the permittivity of the BST films deposited under similar conditions¹¹, fundamental explanations for the decrease in permittivity at small thicknesses must still be sought.

5. RESISTANCE DEGRADATION

Reliability is a crucial aspect in the practical application of advanced dielectrics in DRAMs. Determining the failure mechanism and thereby estimating lifetime is an important aspect of reliability for BST, and a lifetime of 10 years under DRAM operating conditions is desired.

The most important failure mechanism in perovskite thin films is known as "resistance degradation", which manifests itself as a slow increase of the leakage current under a constant E-field after prolonged times. Waser speculates that this type of failure is due to a change of the local defect chemistry between the anode and cathode, which leads to the formation of a forward biased p-n junction.¹²

The lifetime under operating conditions can be extrapolated from the results of accelerated testing conditions under high fields and temperatures. Since resistance degradation is voltage dependent and is thermally activated, a simple Arrhenius relation can be used for either voltage or temperature extrapolations of the time (t_d) required for a one order of magnitude increase of the leakage current after the onset of degradation:

$$t_d = (t_{d_0}) e^{-(Qv(T)/V)} e^{(QT(V)/kT)}$$
 (3)

Figure 2 shows the resistance degradation data obtained at 250°C for fields of 750, 1000 and 1250 kV/cm, for a 24 nm thick Pt/BST/Pt sample. Field-dependent measurements of t_d at different temperatures (200°C, 225°C and 250°C) allowed us to estimate, using Equation 3, the lifetimes at the DRAM operating

condition of 1.6V (Figure 3). The Arrhenius relation above was then used again to extrapolate back to 85°C. As can be seen, the estimated lifetime for films BST films deposited under these conditions is approximately 1300 years, which exceeds the current benchmark of 10 years. Temperature extrapolation of the experimental data to 85°C, followed by voltage extrapolation to 1.6V, gave the same lifetime, indicating consistency between the voltage dependence and the thermally activated character of resistance degradation in BST thin films. This result was for a single sample 24 nm sample, and consistent results have been obtained on thicker samples in that set. Clearly establishing the reliability of thin BST films will require extensive further studies.



Figure 2. J vs. time for 24 nm. BST at high Efields at 250°C.



Figure 3. Extraploted lifetime > 10^3 years for 24 nm. BST at 1.6V.

6. SUMMARY

We have evaluated CVD BST films from 8nm to 30nm thick for use as the capacitor dielectric in ULSI DRAMs. We obtained leakage currents less than 10^{-7} A/cm² at ±1.1V for films as thin as 8 nm, and resistance degradation studies indicate lifetime >10³ years at 1.6V and 85°C for 24 nm BST thin films. Storage density for that thickness was 71 fF/µm², and capacitance for this and thinner films appear to be influenced in part by series capacitance effects.

Acknowledgments

This research has been partially supported by ARPA, through the Ultra-dense Capacitor Processing Partnership, which includes Varian, Micron, IBM, Texas Instruments, IWE Aachen, NCSU and ATMI.

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