Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 800-802

Process Integration of O_3-TEOS CVD SiO_2 for a Cover Film on Ferroelectric Capacitors

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Process effects of the O_3-TEOS CVD SiO_2 cover-film on ferroelectric, $SrBi_2Ta_2O_9$, capacitors are investigated. The formation of cover film degrades the ferroelectric characteristics. The degradation of the remnant polarization (2Pr) is related to the deposition temperature, eventually the water-content level in the covered film. The breakdown voltage (V_b) degradation, however, always occurs irrespective of the deposition temperature. These degradations of the remnant polarization and the breakdown voltage are recovered by the 600°C-post-annealing, resulting in 2Pr=15μC/cm^2 and V_b>10V for the 180nm-thick, $SrBi_2Ta_2O_9$ film with the 400nm-thick, O_3-TEOS cover film.

1. INTRODUCTION

In ferroelectric memory fabrication process, one of the key processes is a cover-film formation on ferroelectric capacitors without any degradation of ferroelectric characteristics. The cover-films, basically SiO_2 films, are obtained by several CVD technologies such as plasma-CVD with SiH_4/O_2 gas or $TEOS/O_2$ gas, or thermal-CVD with SiH_4/O_2 gas or $TEOS/O_3$ gas. The selection among these CVD technologies is very important to accomplish the cover-film formation process.

Ferroelectric characteristics were degraded by plasma damage[1] or by deoxidation of ferroelectric film in reduction ambience such as W-CVD process[2]. Therefore, plasma-CVD process as mentioned above is inadequate for the cover-film. Considering mega-bit class ferroelectric memories[3,4], the step coverage of interlayer dielectrics such as the cover-film will be also very important. The silicon oxide by thermal-CVD with SiH_4/O_2 gas, which has poor step coverage such as overhang shape, is also inadequate as the future interlayer dielectrics. The O_3-TEOS CVD process proceeds basically in oxidative ambience and shows good step coverage, and is a promising candidate for the cover-film. But the O_3-TEOS film contains water, which influences the ferroelectric characteristics. The content of water is controlled by the substrate-temperature during the CVD as well as the post-annealing.

The other candidate is a sputter SiO_2 of dense and water- and chemical-free characteristics, but the step coverage is poor. Then, we propose the O_3-TEOS/sputter SiO_2 structure, as shown in Figure 1. The combination of the O_3-TEOS and the sputter SiO_2 is expected to have good step coverage over the capacitor and also to suppress the degradation of ferroelectric characteristics. In this report, the effects of the O_3-TEOS CVD properties on the $SrBi_2Ta_2O_9$ capacitors are examined in the O_3-TEOS/sputter SiO_2 structure.

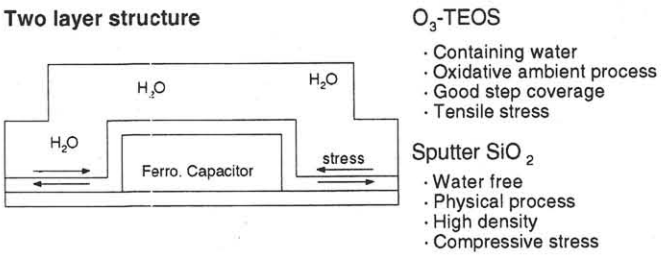

Fig.1 Concept of O_3-TEOS/sputter SiO_2 structure.

2. EXPERIMENTAL

Figure 2 shows sample fabrication process flow. A simple ferroelectric capacitor structure was fabricated by a simple process : A Ti adhesion layer and a Pt (200nm) bottom electrode layer were sputtered on the SiO_2/Si substrate. A 180nm-thick, $SrBi_2Ta_2O_9$ film was coated by MOD (Metal Organic Deposition) process on the Pt/Ti. A top electrode layer of Pt (200nm) was sputtered on the $SrBi_2Ta_2O_9$ film. The layers of Pt/$SrBi_2Ta_2O_9$/Pt/Ti were patterned by ion milling with photoresist mask. The top

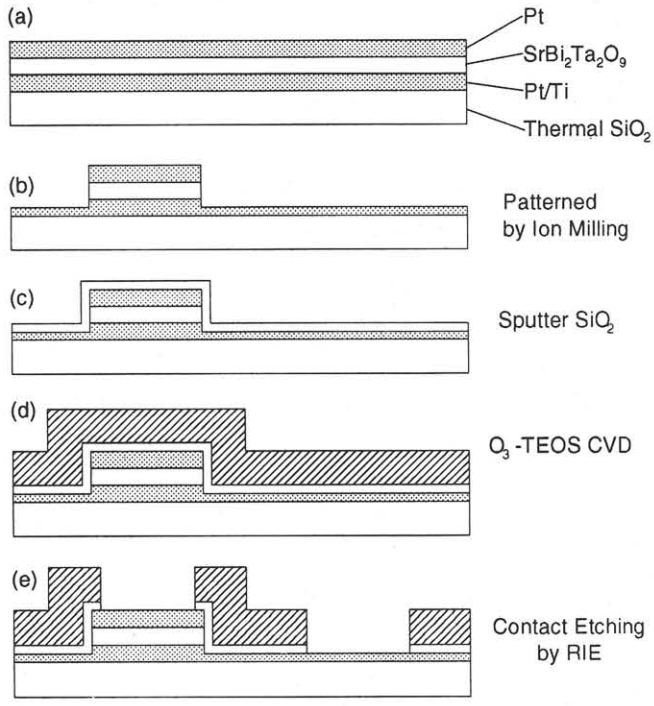

Fig.2 Process flow of the ferroelectric capacitor covered with O_3-TEOS/sputter SiO_2 structure.

electrode size of the capacitor was 100μm×100μm. A 100nm-thick sputter-SiO_2 was deposited by RF sputtering with Ar plasma. Then, the 400nm-thick, O_3-TEOS films were deposited by an atmospheric pressure CVD (APCVD) system with 70g/Nm^3 O_3-concentration at the substrate temperature (Ts) of 300°C or 450°C. Contact holes were formed by RIE with CHF_3 plasma. The plasma damage of the contact etching may influence ferroelectric characteristics. In this experiments, the plasma etching condition is a constant to keep the plasma damage a constant level for all samples. The size of contact halls were large as 80μm×80μm to measure ferroelectric characteristics directly without conventional Al metallization. Some of samples were annealed in N_2 at 400°C or 600°C after the contact-hole formation (the post-annealing process). Water contents in the films were estimated by Fourier transformed infrared spectroscopy (FT-IR)[5,6]. The ferroelectric characteristics such as the remnant polarization (2Pr) and the leakage current were measured for the samples of the coverless capacitor shown in Figure 2(b), and the covered capacitors shown in Figure 2(e) with or without the post-annealing.

Figure 3 shows the cross sectional SEM image of the ferroelectric capacitor covered with O_3-TEOS/sputter SiO_2 structure. Left image is the edge of contact hall, right image is the edge of capacitor. O_3-TEOS CVD film has good step coverage.

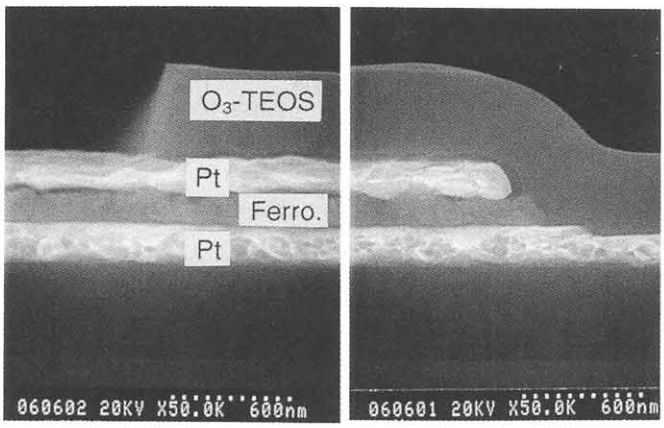

Fig.3 The cross sectional SEM image of the ferroelectric capacitor covered with O_3-TEOS/sputter SiO_2 structure.

3. RESULTS AND DISCUSSION

Figure 4 and figure 5 show the hysteresis loop of the coverless capacitor and loops of the capacitors covered with O_3-TEOS films deposited at 300°C or 450°C, respectively. As comparing the hysteresis loops of the covered capacitors with that of the coverless one, the loop shapes of the covered capacitors were broader than that of the coverless one, indicating that the ferroelectric properties were degraded by the O_3-TEOS/sputter SiO_2 film deposition. The hysteresis loop shape of 300°C covered capacitor was broader than 450°C covered.

Figure 6 shows remnant polarization for coverless capacitors and covered capacitors with O_3-TEOS films deposited at 300°C or 450°C. The degradation of remnant polarization of the 300°C and the 450°C covered films was -35% and -10%, respectively. Since the water contents of O_3-TEOS films deposited at 300°C and 450°C are 4.6wt% and 0.7wt%, respectively, meaning that the degradation of 2Pr is related to the water-content level in the covered film. Namely, the O_3-TEOS film of higher deposition temperature such as 450°C is desirable. A part of the 300°C covered films was peeled off from the edges of capacitors during as contact hole fabrication process due to the film shrinkage with a large amount of water included[7].

Figure 7 shows the leakage current of coverless capacitors and capacitors covered with O_3-TEOS films deposited at 450°C. The breakdown voltage of coverless capacitors was over 10V. After the cover film deposition and the contact halls formation, the breakdown voltage decreased to 2V. Even though the 450°C covered film with only 0.7wt%-water was used, the leakage current characteristics degraded very much. The degradation of breakdown voltage occurred irrespective of the deposition temperature. Therefore, the degradation of breakdown voltage is caused by not only water in the cover film but also other reason, such as plasma damage during contact hole formation.

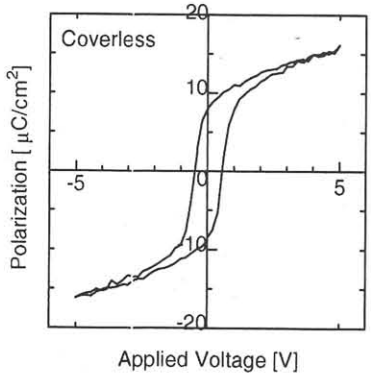

Fig.4 Hysteresis loop of coverless capacitor.

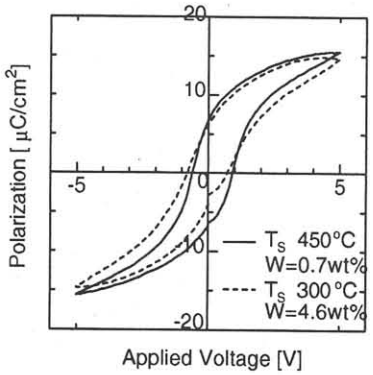

Fig.5 Hysteresis loop of covered capacitors with O_3-TEOS/sputter SiO_2. The "W" is the water content in O_3-TEOS SiO_2 film.

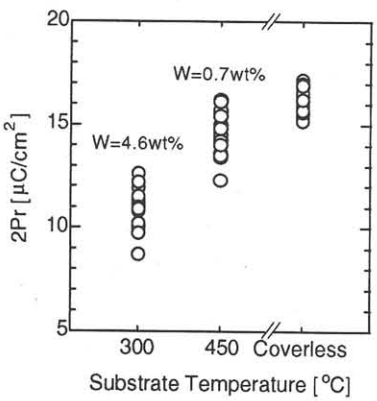

Fig.6 Remnant polarization for coverless and covered capacitors with O_3-TEOS/sputter SiO_2.

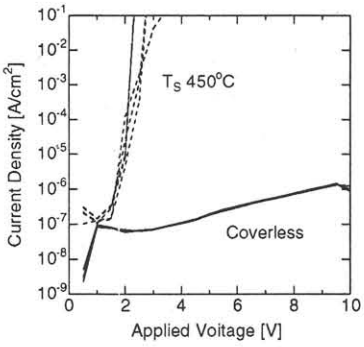

Fig.7 Leakage current of coverless capacitors and covered capacitors with O_3-TEOS/sputter SiO_2.

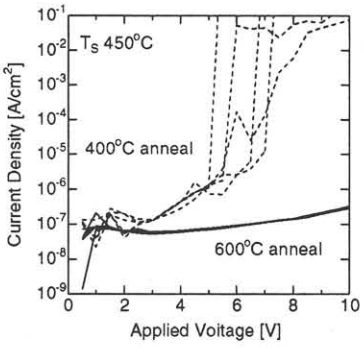

Fig.8 Leakage current of covered capacitors with O_3-TEOS/sputter SiO_2 films with 20-min. annealing at 400°C or 600°C in N_2.

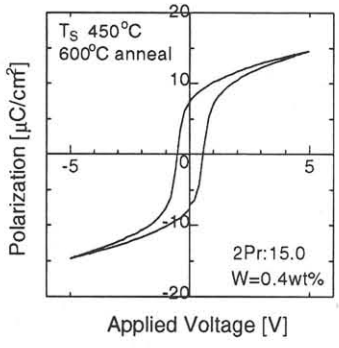

Fig.9 Hysteresis loop of covered capacitor with O_3-TEOS/sputter SiO_2 film with 20-min. annealing at 600°C in N_2.

Figure 8 shows the leakage current of covered capacitors with O_3-TEOS/sputter SiO_2 films, which were deposited at 450°C and annealed for 20minutes at 400°C or 600°C in N_2. The post annealing at 400°C, which was lower than the O_3-TEOS film-deposition temperature, was not enough to recover the degraded breakdown voltage. By the 600°C post-annealing, the water content in the film decreased to 0.4wt%, and the breakdown voltage was recovered over 10V. Figure 9 shows hysteresis loop of covered capacitor with O_3-TEOS/sputter SiO_2 film, which was deposited at 450°C and annealed in N_2 for 20minutes at 600°C. The hysteresis loop of covered capacitor with post-annealing at 600°C was the same shape as that of the coverless capacitor. Hysteresis characteristics also recovered by 600°C anneal.

4. SUMMARY

Process effects of the O_3-TEOS CVD condition and the post-annealing on the ferroelectric characteristics were investigated. The O_3-TEOS film, which contained water, degraded the ferroelectric characteristics. The degradation of the remnant polarization is related to the deposition temperature, eventually the water-content level in the covered film. And the breakdown voltage of the covered O_3-TEOS/sputter SiO_2 structure also degraded. The degradations of the breakdown voltage and the remnant polarization were recovered by the 600°C-post-annealing. As the result, the remnant polarization was 15μC/cm^2 and the breakdown voltage was over 10V for 180nm-thick, $SrBi_2Ta_2O_9$ film with the 400nm-thick, O_3-TEOS cover film.

In conclusion, the post-annealing for the O_3-TEOS/sputter SiO_2 film diminishes the damages during the cover-film formation, and is utilized for ferroelectric memory fabrication process with good step coverage over the capacitor.

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