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Side Gate Single Electron Transistor with Multi-Islands Structure Operated at Room Temperature Made by STM/AFM Nano-Oxidation Process

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A single electron transistor(SET) with a side gate electrode and a multi-islands structure was fabricated using the STM/AFM nano-oxidation process. The clear Coulomb gap and Coulomb staircases with a period of 160mV and Coulomb oscillation with a period of 406mV are obtained even at room temperature for the first time owing to the suppression of the co-tunneling effect by multi-tunnel junctions and to effective side gate bias.

1. Introduction

For the room temperature operation of single electron transistor (SET), the size of an island and a tunnel junction must be as small as possible, and the total capacitance of the SET should be less than 1aF. The fabrication process how to realize the nano-meter order size is an important problems. In the previous work, we have established the new nano-meter order fabrication process which adopted the selective anodization process using the STM tip/AFM cantilever as an infinitesimally small cathode1,2), and the nano-meter order oxidized metal line which works as an energy barrier for an electron was obtained. Using this STM/AFM nano-oxidation process, the SET with two islands and back gate structure was fabricated, and the room temperature operation of the SET was accomplished [3,4]. However, there still remains two problems in this SET. One is that though the SET showed the clear Coulomb staircase, the SET could not show the clear Coulomb gap owing to the large co-tunneling leak current due to the small number of the tunneling junctions. The other is that the SET could not show the clear Coulomb oscillation because of the poor gate bias effect which was applied far from the back side of the Si substrate. In order to solve these problems, the new structure SET with a side gate and a multi-islands structure was fabricated. The side gate SET with a multi-islands structure shows the clear Coulomb gap and staircase as well as the clear Coulomb oscillation at room temperature.

2. Structure of Side Gate SET

The structure of the side gate SET with multi-islands structure is schematically shown in Fig. 1. The substrate is thermally oxidized SiO_2(100nm) / n type silicon, and 3nm thin titanium (Ti) layer is deposited on it. Using the STM tip and/or AFM conductive cantilever as a cathode, the surface of the Ti layer is oxidized by the anodized chemical reaction through the water that adhered to the surface of the Ti from the ambient air[1,2]. Then the oxidized narrow Ti (TiO_x) line is formed selectively just under the STM tip and/or AFM cantilever. The TiOx layer has a resistivity of about seven orders of magnitude higher value than that of the Ti layer, and therefore could work as an energy barrier for an electron flow[2]. Two large TiO_x barriers in Fig. 1 work as a gate barrier and a source-drain barrier, respectively. Between these two large barriers, several narrow tunnel junctions are formed and island regions are formed between them. Thus, the gate electrode is set just near the island region of the SET. The five islands SET and two islands SET were fabricated in the experiment. In Fig. 1, the structure of the two islands SET is shown. Figure 2 shows the AFM image of the fabricated side gate SET with five islands structure. The width of the TiOx gate barrier is relatively wide value of 430nm to completely suppress the gate leak current to the source-drain current. The width of the TiOx gate barrier could be reduced to about 200nm wide to increase the gate bias effect to the island without the fear of the gate leak current. The width of the TiOx source-drain barrier is as wide as 940nm to completely stop the direct leak electron flow from the source Ti metal to the drain Ti metal. Between the TiOx gate barrier and the source-drain barrier, the six narrow TiOx lines are seen which works as tunneling junctions of SET. The five islands are formed between these six tunneling junctions. The size of the six

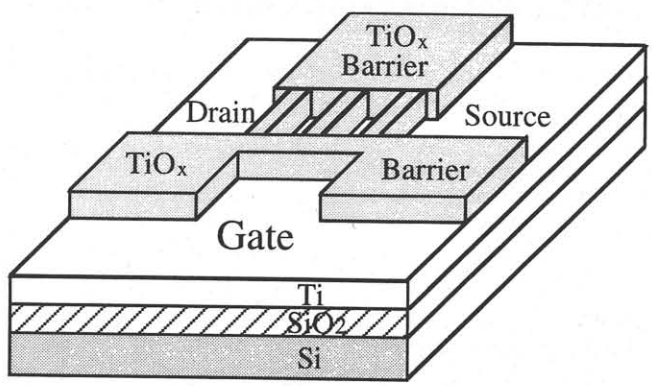

Fig. 1, Schematic illustration of side gate SET with multi-islands structure.

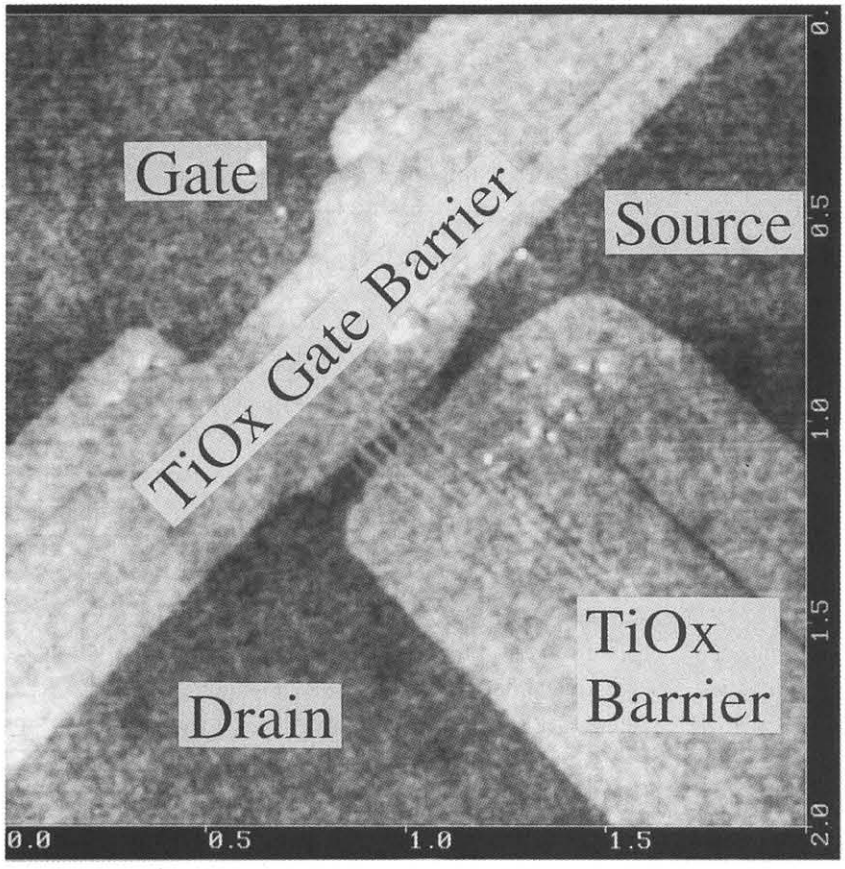

Fig. 2, AFM image of fabricated side gate SET with 5 islands structure.

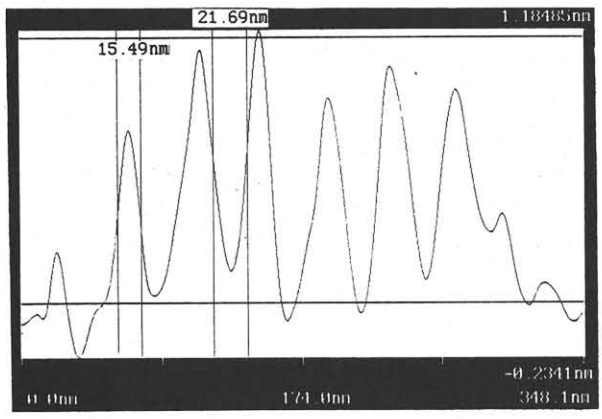

Fig. 3, Size of tunneling junctions and islands.

tunnel junctions and five islands between them are measured by AFM and is shown in Fig. 3. The typical size of the tunneling junction is 15nm wide and that of the island is 21nm wide, respectively. The energy barrier height between TiOx and Ti metal system measured by the temperature dependence of the current of the planar type Ti/TiOx line/Ti system is 0.308eV[3]. Therefore, the tunneling junction width of 15nm is thin enough for electrons to tunnel through it. The width between the TiOx gate barrier and the source-drain barrier is 40nm which define the length of the tunneling junctions and the another size of the island.

3. Electrical Characteristics

Figure 4 shows the drain current-drain voltage characteristics of the side gate SET with 5 islands structure at room temperature with the gate terminal kept open. The clear Coulomb gap of about 160mV is seen at around zero drain voltage. There is no leak current seen in the Coulomb gap. This may be attributed to the multi-tunneling junctions which can drastically decrease the co-tunneling current[5]. The Coulomb staircases with almost the same periods are also obtained even at room temperature. The first Coulomb

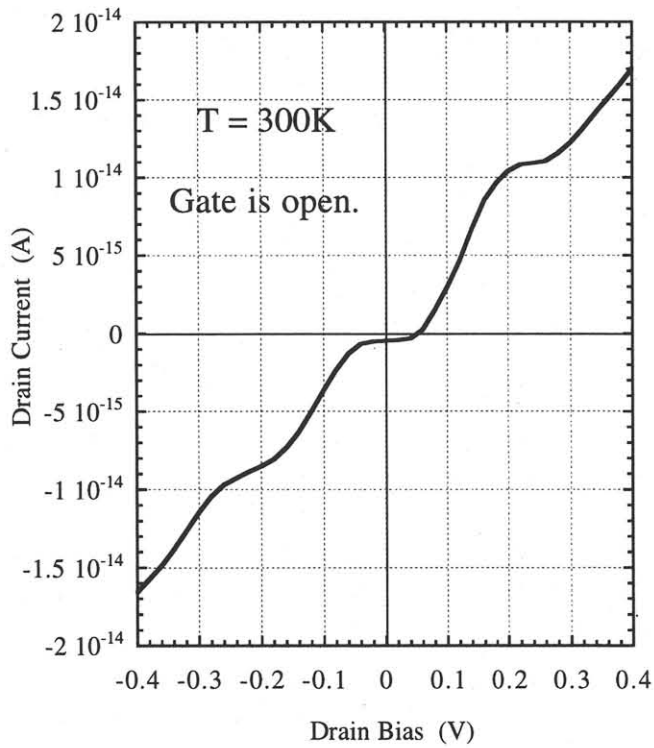

Fig. 4, Drain current -voltage characteristics of SET with 5 islands structure at 300K. Gate is kept open. Coulomb gap and Coulomb staircase of ~160mV periods are observed.

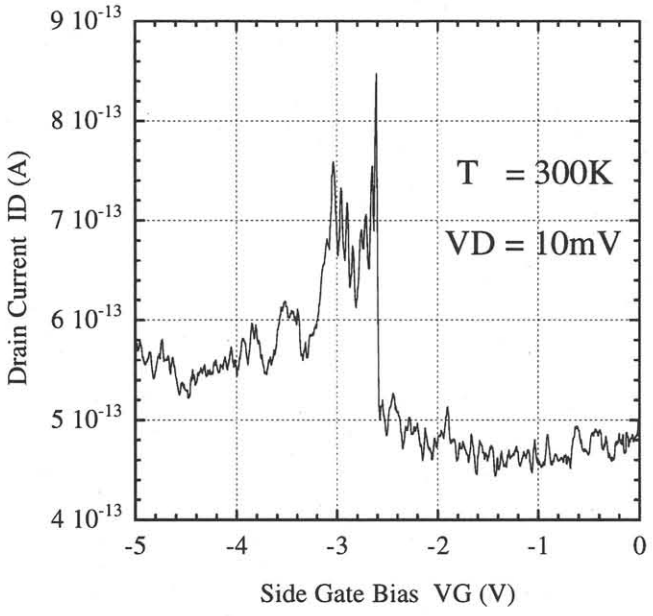

Fig. 5, Gate bias dependence of drain current at 300K for side gate SET with two islands structure. Drain bias is kept to be V_D = 10mV. Four Coulomb oscillation peaks are observed.

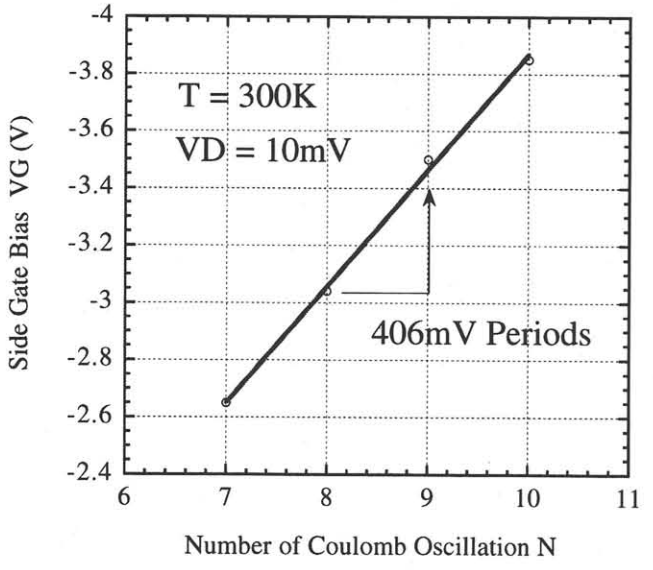

Fig. 6, Periods of Coulomb oscillation.

staircase at +180mV and -180mV are clearly seen. The total capacitance of the SET estimated from the periods of Coulomb gap is C_Σ = ~1aF. A current offset of about-5x10-16A at zero drain voltage may be owing to the measurement error in the range of so small drain current.

The gate bias dependence of the drain current of the side gate SET with three tunneling junctions and two islands structure was examined at room temperature and is shown in Fig. 5. The drain bias was set at V_D=10mV and the gate bias was changed from 0V to -5V. The four large oscillation of the current was seen at around the gate bias of V_G= -2.7V, -3.1V, -3.5V, -3.9V. The each peaks fits on the linear line as shown in Fig. 6. Therefore, this current oscillation could be concluded to be the Coulomb oscillation with period of 406mV. From this period of the Coulomb oscillation, the gate capacitance of the side gate SET is calculated to be Cg=~0.4aF. The reason why there are no Coulomb oscillation observed between the gate bias of Vg=0V and -3.6V is not clear.

4. Conclusion

Using the STM/AFM nano-oxidation process, the side gate SET with multi-islands structure was fabricated. The SET shows the clear 160mV Coulomb gap with no leak current at room temperature for the first time owing to the suppression of the co-tunneling leak current by the multi-tunneling junctions. The Coulomb oscillation with the periods of 406mV was also obtained at room temperature owing to the effective side gate structure. The side gate structure SET is the promising device for the more complicated SET circuit such as memorys and logics.

Reference

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