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High-Temperature Operation of $Al/Al_2O_3/Al$ Single-Electron Transistors

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We report two novel techniques for fabricating high-temperature operating Al-based single-electron transistors (SETs). One is the Anodization Controlled Miniaturization Enhancement (ACME). Utilizing anodization of Al electrodes, we reduced the size of tunnel junctions prepared with standard e-beam lithography. This process enhanced the charging energy of an SET by nearly 10 times. The other is a modified shadow evaporation. By this technique, we made SETs with a 20-nm island which showed periodic gate modulation up to above 100 K.

1. INTRODUCTION

To put an extra electron on a small metallic island, that is, to charge up the island by a charge e, one needs to supply charging energy $E_C=e^2/2C_\Sigma$, where C_Σ is the total capacitance seen from the island. This energy results in the correlated electron transport in single-electron devices, unless either the quantum fluctuation through the tunnel junctions $\sim\hbar RC$ (R and C are the resistance and the capacitance of the junction) or the thermal fluctuation $\sim k_BT$ exceeds E_C.[1] Thus, the operating temperature of single-electron devices is limited by the charging energy and it was restricted to cryogenic temperature in the early stage of the research which started about a decade ago. Since E_C is mainly determined by the device geometry, for a higher-temperature operation of single-electron devices, it is necessary to fabricate smaller islands and smaller junctions.

Along this way, many works have been reported. Some of them utilized naturally-formed nano-grains as small islands.[2),3)] In spite of the fact that it is usually difficult to control the variation of grains, several authors reported the electron transport via a single grain.[4),5)] Using an STM tip adjusted right above a small metallic particle, the Coulomb staircase, which is an evidence of correlated electron transport, was observed at room temperature.[6)] Others fabricated single-electron devices which consisted of intentionally-made islands and junctions. Finely patterned SIMOX structure with thermal oxidation was shown to produce two tunnel junctions and an island. The gate modulation of such devices was observed nearly up to room temperature.[7)] An STM nano-oxidation process was also used to fabricate high-temperature operating single-electron devices.[8)]

Despite of the many works on high-temperature single-electron devices described above, periodic gate-voltage modulation of the current in a single-electron transistor (SET), which is one of the most important feature of single-electron devices, was not clearly seen in most of those devices. This is in contrast to the Al-based SETs (usually working below 1 K) which show perfectly periodic gate modulations repeatedly. We believe that the high carrier density in the Al electrodes and the high tunnel barrier in the Al-oxide tunnel junction are important in such ideally periodic modulation. However, the operation of the metallic SETs were usually restricted to deep cryogenic temperature owing to the difficulty in the nano-fabrication technology. Here we report two newly developed methods to fabricate high-temperature operating Al-based single-electron transistors and their periodic gate modulation.

2. ANODIZATION CONTROLLED MINIATURIZATION ENHANCEMENT

It is generally accepted that the organic polymer resists for e-beam lithography have a resolution limit around 10 nm. Hence one of the recent approaches for nanofabrication is to combine e-beam lithography with a further miniaturization technique.[7)] Ideally, such additional process should have a better resolution, and should be controllable with external parameters.

We tried anodization of Al as the additional miniaturization process and successfully decreased the size of $Al/Al_2O_3/Al$ tunnel junctions prepared by the standard e-beam lithography and two-angle shadow evaporation.[9)] The advantages of this method are as follows. (i) The anodization process (thickness) can be controlled by the applied voltage between the single-electron device (anode) and the cathode. (ii) During the miniaturization, we can monitor the progress by *in situ* measurement of the conductance of the device. (iii) Miniaturization by the

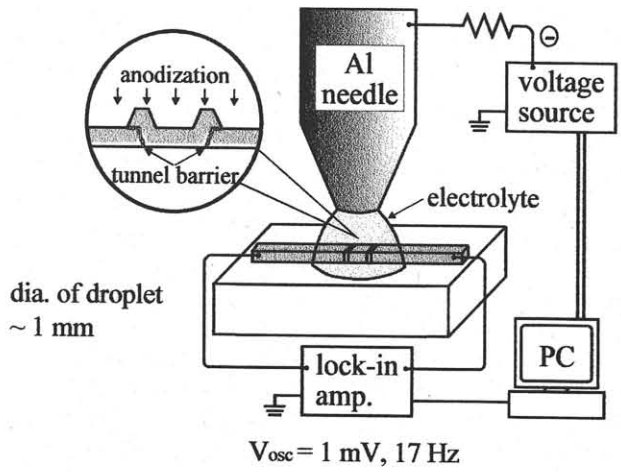

Fig. 1. A schematic of the setup of ACME. The inset shows a blowup of the tunnel junctions, where the gray area indicates anodized part of the electrodes.

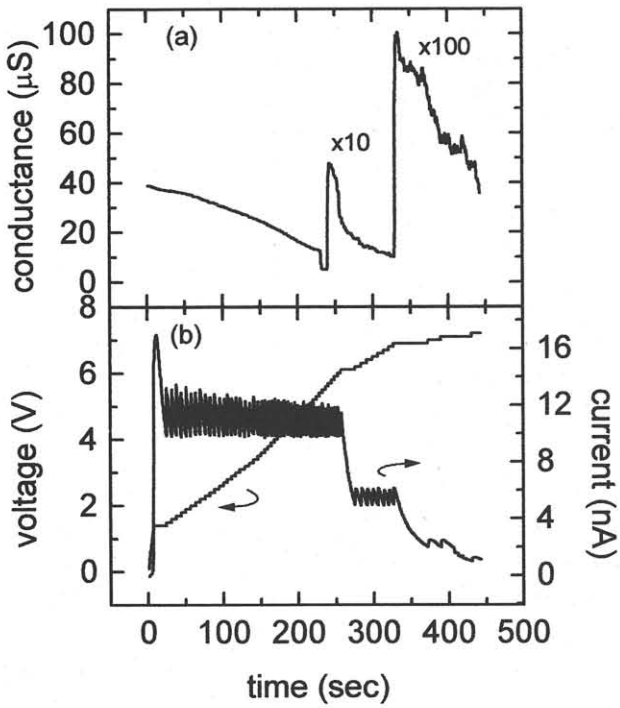

Fig. 2. (a) Conductance of an SET and (b) anodization voltage and current during the ACME process.

anodization does not degrade the quality of the tunnel barrier but simply reduces the effective size of the junctions. The high-quality Al_2O_3 tunnel barrier of the junctions are formed by oxidation in a controlled O_2 atmosphere during the shadow evaporation method.

Figure 1 shows schematically the setup of our Anodization Controlled Miniaturization Enhancement (ACME) technique.[10] We prepared an SET with a 300-nm island on a Si substrate covered with an oxidized layer. The SET had tunnel junctions of an area 40×40 nm^2 and its charging energy was estimated to be about 0.5 meV. Then we put a droplet of electrolyte between the SET (as the anode) and an Al needle (as the cathode). The surface of the SET was anodized and the effective area of tunnel junctions was decreased with the increase in the applied anodization voltage. This mechanism is illustrated in the inset of Fig. 1. An example of the evolution of the anodization parameters during the process is shown in Fig. 2. The voltage was set by a computer so as to keep the anodization current close to the desired value (10 nA at first, then switched to 5, 2, 1 nA, sequentially). A high current should be avoided because it will degrade the quality of the anodized oxide. After the ACME, the conductance of the SET could be made as small as one hundredth of the initial value. The details of the process has been published in Ref. 10.

We measured current vs. gate-voltage (I-V_g) characteristics of SETs after the ACME. It showed periodic gate modulation up to nearly 30 K. Analysis of current-voltage (I-V) curves gave their charging energy of about 4 meV. This enhancement of E_C (5-10 times of the initial value) was not as large as the enhancement of the resistance (~100 times) for many of our samples. We attributed this limitation of the enhancement to the asymmetry of the initially prepared junctions as well as the self capacitance of the island. In our samples, the spread in junction area was about 20%, which would limit the enhancement of E_C to about 10 times. The self capacitance of the 300-nm island was also estimated to be comparable with the total capacitance of island after the ACME.

3. THREE-ANGLE SHADOW EVAPORATION

As we denoted above, in ACME we could decrease the junction capacitance effectively but the residual capacitance after ACME would ultimately limit the operating temperature of the device. Part of the residue seems to be the self capacitance of the island. However, ACME is not capable of reducing the self capacitance because the self capacitance is mainly determined by the longest dimension of the island, that is, the length of the island. ACME do not shorten it so much but just decreases the width and the thickness of the island. Hence, we moved back to the lithography and tried to fabricate a much shorter island.

One of the limits in the fabrication of a short island in the standard two-angle evaporation method is the creation of a very narrow hanging bridge mask. The length of the island can not be shorter than the width of the bridge which is typically wider than 50 nm in our lithography process. To overcome this problem, we used three-angle shadow evaporation. A layout of the evaporated pattern is shown in Fig. 3(a) with an SEM photograph in Fig. 3(b). Using this technique, we could make an SET with a 20-nm island.[11]

Figure 4 shows the I-V_g curve of an SET with a 20-nm island at 4.2 K. It shows a periodic gate modulation without any background current. The modulation was perfect in the sense that the mean current did not drift with the gate

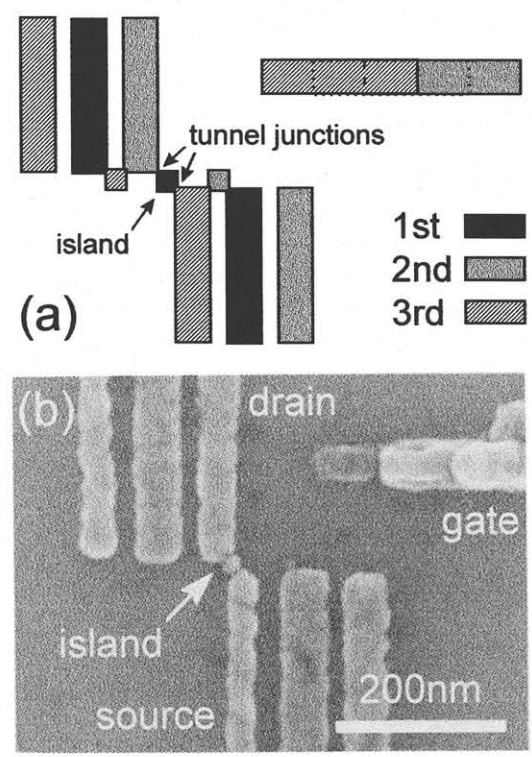

Fig. 3. (a) A schematic layout of the three-angle shadow evaporation. (b) An SEM photograph of an SET with a 20-nm island.

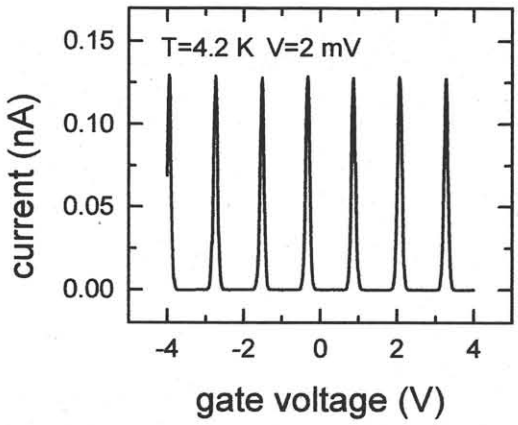

Fig. 4. An I-V_g curve of an SET with a 20-nm island at 4.2 K. The applied source-drain voltage was 2 mV.

voltage, indicating that the tunnel barrier was not affected by the gate voltage. The modulation was very close to that the orthodox theory predicted.[1] This sample had a charging energy of 11.4 meV which corresponded to ~130 K. The temperature dependence of I-V_g curves is also shown in Fig. 5. Even above 100 K, the periodic gate modulation survived, though the modulation of current was small (~0.5% at ~100 K, ~3% at ~77 K).

We also tried ACME on the SETs with a 20-nm island. In this case, the size of the tunnel junctions was so small (~10 × 10 nm^2) that the variation in size was large. Although the resistance of the SET was increased by about 10-50 times after ACME, the enhancement of E_C was only about 20%, which was small compared with the case of the SET with a larger island. We believe that in an SET with a 20-nm island, the total capacitance of the island was dominated by the parasitic capacitance rather than the junction capacitance; the latter would scale with junction resistance.

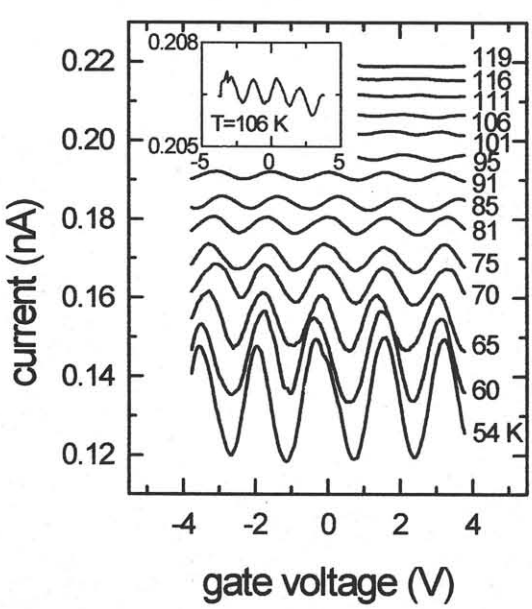

Fig. 5. Temperature dependence of I-V_g curves of the same device as in Fig. 4. The applied source-drain voltage was 2 mV.

4. SUMMARY

We report two novel techniques for fabricating ultrasmall Al-based single-electron transistors: Anodization Controlled Miniaturization Enhancement and the three-angle shadow evaporation. The former technique was useful for increasing the charging energy of an SET when the junction capacitance dominated the total capacitance of the island. By the three-angle shadow evaporation, we made an SET with a 20-nm island and demonstrated a periodic gate modulation up to above 100 K.

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