Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 455-457



# Coulomb Blockade Effects in Edge Quantum Wire SOI MOSFETs

**Akiko Ohata and Akira Toriumi**

**ULSI Research Laboratories, Toshiba Corporation**
**1, Komukai Toshiba-cho, Kawasaki 210, Japan**

## Abstract

An edge quantum wire SOI-MOSFET has been fabricated, measured and analyzed. In this device, clear Coulomb oscillations can be observed, which are caused by multi-junction system in the quantum wire channel. By addition of another gate to this structure, the phase of Coulomb oscillations can be tuned by adjusting the SOI body potential. This method may solve the critical problem of the fixed or mobile trapped electrons near SET devices.

## 1. Introduction

Single electron charging effects have attracted attention, since they provide a possibility for future ultra-low-power devices. Furthermore, the research of silicon (Si) single electron tunneling (SET) device[1),2),3)] is very challenging because of material stability, process controllability, or possible hybridization with classical silicon devices such as high performance CMOS.

We have proposed a device concept of Si SET devices hybridized with CMOS[4)], in which the external world can only see CMOS, and the low gain SET devices will be compensated by conventional CMOS performance.

We have already fabricated Si SET device with $Si/SiO_2/Si$ junctions. In this device, for reducing the tunneling area, we defined the size by the thickness control of polycrystalline Si film[5)], which can overcome the size limitation determined by lithography. On the other hand, it is expected that ultimately narrow channel MOSFET[4)] can be realized using the method, which is known as the edge Q1D in the ultra-thin compound semiconductor heterostructure[6)]. However, to our knowledge, there have been no reports on the Si edge quantum wire MOSFET except a few reports on the Si bulk quantum wire MOSFET[7),8)].

In this paper, we report experimental results of the electron transport in edge quantum wire (EQW) MOSFET fabricated on ultra-thin SOI, where we found clear Coulomb oscillations of the channel current with gate voltage sweeping. Furthermore, we demonstrate the phase tuning of Coulomb oscillations by modifying the device structure.

## 2. Device Structure and Performance

The ultra-thin SOI film was formed by local oxidation of SIMOX wafer. Only the channel region was thinned to reduce source/drain parasitic resistance[9)]. Edge region was fabricated by reactive ion etching and gate electrode was formed only at the side wall of EQW in order to form inversion layer only at the side edge as shown in Fig.1. The actual thickness of SOI film becomes finally less than 15nm. Thus, the width of EQW becomes narrower than 15nm.

The device was measured using two probe DC method. At 4.2K, clear oscillations in the gate voltage dependence of channel current are observed as shown in Fig. 2. In some devices, these oscillations are observable even at 77K. These oscillations are not always periodic in wide gate voltage sweeping. However, it should be noticed that, at higher gate voltage region, the current is rather periodically modulated by the gate voltage sweeping. The gate voltage providing each peak shows clear periodicity as shown in Fig. 3. Considering the results of clear periodic oscillations at high gate voltage region, it is reasonable to suppose that conductance oscillations are caused by CB effects in the channel with multi-junctions formed by several unintentional potential barriers. The periodicity is quantitatively determined as 70mV, which means that the gate capacitance between gate electrode and isolated electrode is 2aF, and that the length of isolated region is 0.1μm, assuming the parallel plate capacitor model. This is a reasonable length considering the channel length in our devices. Furthermore, in the drain voltage dependence of channel current, non-linear structure was observed and periodically modulated by the applied gate voltage as shown in Fig. 4. This is another evidence for CB effects in the electron transport in this device.

Furthermore, we considered one dimensional size effects of the EQW as a possible origin of the current oscillations by measuring the magnetic field dependence of the conductance. Figure 5 shows the gate voltage dependence of the channel current as a parameter of magnetic field. It shows that an overall behavior of oscillations do not depend on the magnetic field at 0.3K. This fact shows that quantum size effect is not important for the electron transport in this device.

## 3. Double Gate EQW Structure

The phase randomness of Coulomb oscillations is an operational instability issue[10)]. For tuning it, we propose a double gate (DG)-EQW SOI-MOSFET. One gate, which is called the front gate as shown in Fig. 6, is used to create the inversion layer, as described in the previous section. The other gate, which is called the back gate, is used to tune the threshold voltage from the back side of the edge channel surface. In other words, the front gate controls the electron number of the Coulomb island and the back gate controls the substrate potential of the SOI film. Figure 6 shows the front gate voltage dependence of

channel current as a parameter of the back gate voltage. We note here that the phase of the oscillating channel current is changed by $2\pi$ with applying a small back gate voltage. It shows that the phase of Coulomb oscillations can be tuned by the back gate, and that the DG-EQW is rather robust against the external disturbance due to fixed or mobile trapped electrons.

## 4. Summary and Future Prospects

We fabricated Si-EQW, the width of which was determined by the thickness of SOI film. The results have shown a promising fact that the Q1D structure is sensitive to the small potential modulation on the channel. By introducing intentional tunneling barriers, it will be possible to make SET devices with gate controllable tunnel barriers. Furthermore, it is noted that EQW SOI-MOSFET is fabricated by conventional CMOS process as described above. This suggests that EQW SOI-MOSFET can be hybridized with conventional MOSFET and that CB effects can be detected by the normal SOI-MOSFET on a same chip. In fact, we fabricated a normal n-channel MOSFET coupled with EQW MOSFET. The detection of Coulomb blockade signal by normal MOSFET is now under investigation.

Therefore, EQW structure with intentional potential barriers will be a possible structure for the future single electron devices.

**Acknowledgments**

The authors would like to thank H. Niiyama, M. Takahashi, S. Satake, M. Iwase, and K. Uchida for their useful discussion.

This work was performed under the management of FED as a part of the MITI R&D program ( Quantum Functional Devices ) supported by NEDO.

**References**

1) K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, Tech. Dig. of IEDM 94, 541.
2) Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Tech. Dig. of IEDM 94, 938.
3) E. Leobandung, L. Guo, and S. Y. Chou, Tech. Dig. of IEDM 95, 367
4) A. Toriumi, A. Ohata and J. Koga, Extended Abstracts of 14th symposium on FED (1995) 67, Tokyo.
5) A. Ohata, H. Niiyama, T. Shibata, K. Nakajima and A. Toriumi, Jpn. J. Appl. Phys. **34** (1995) 4485.
6) H. Sakaki, Jpn. J. Appl. Phys. **19** (1980) L735.
7) K. Morimoto, Y. Hirai, K. Yuki, K. Inoue, M. Niwa, and J. Yasui, Extended Abstracts of 1993 S.S.D.M. (1993) 344, Makuhari.
8) H. Ishikuro, T. Fujii, T. Saraya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, Extended Abstracts of the 43rd Spring Meeting, The Japan Society of Applied Physics and Related Societies (1996) 26P-ZA-12.
9) A. Toriumi, J. Koga, H. Satake and A. Ohata, Tech. Dig. of IEDM 95, 847
10) D. V. Averin and K. K. Likharev, in Single Charge Tunneling, ed. By H. Grabert and M. H. Devoret (Plenum, New York, 1992),311

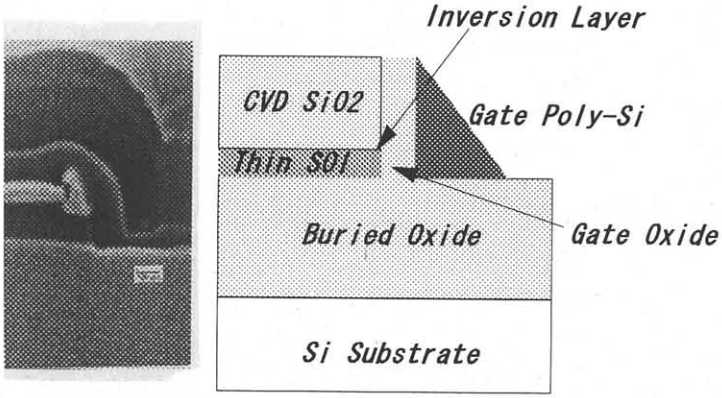


Fig.1 SEM picture and schematic view of the cross-section of edge quantum wire SOI MOSFET. The SOI film thickness is less than 15nm. The channel length is determined by the phosphorous diffused area implanted for source and drain region.

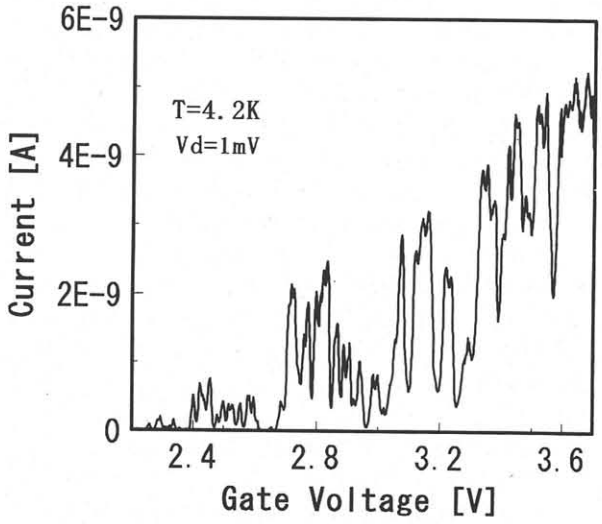


Fig.2 Gate voltage dependence of channel current near the threshold.
In this case, channel lendth is about 3.5μm.

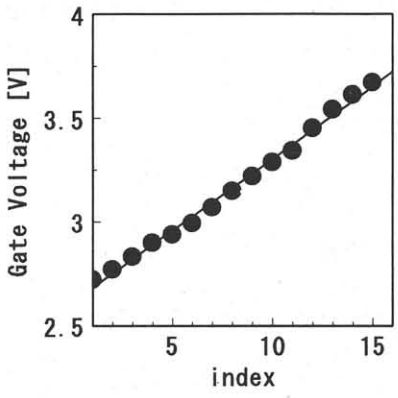


Fig.3 The gate voltage for peak index at the higher gate voltage region in Fig.2.

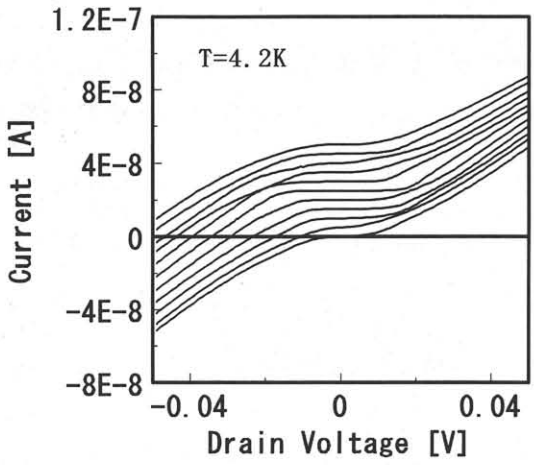


Fig.4 Drain voltage dependence of channel current with changing gate voltage as on →off→on in Fig.2. The current level is offset for clarity.

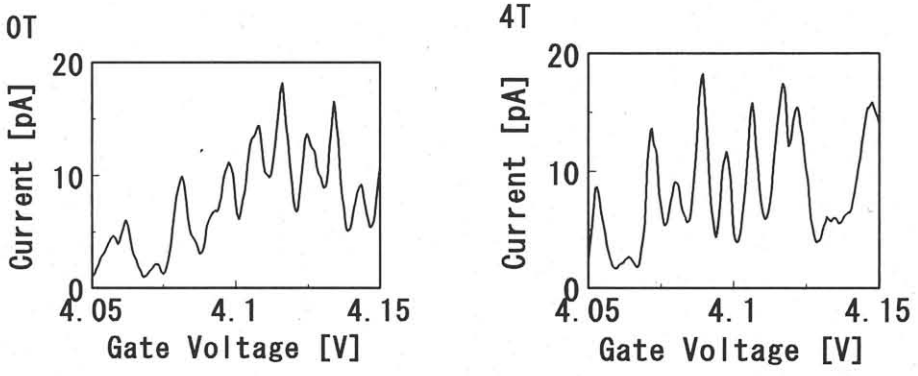


Fig5. Gate voltage dependence of channel current as a parameter of magnetic field. (T=0.3K)

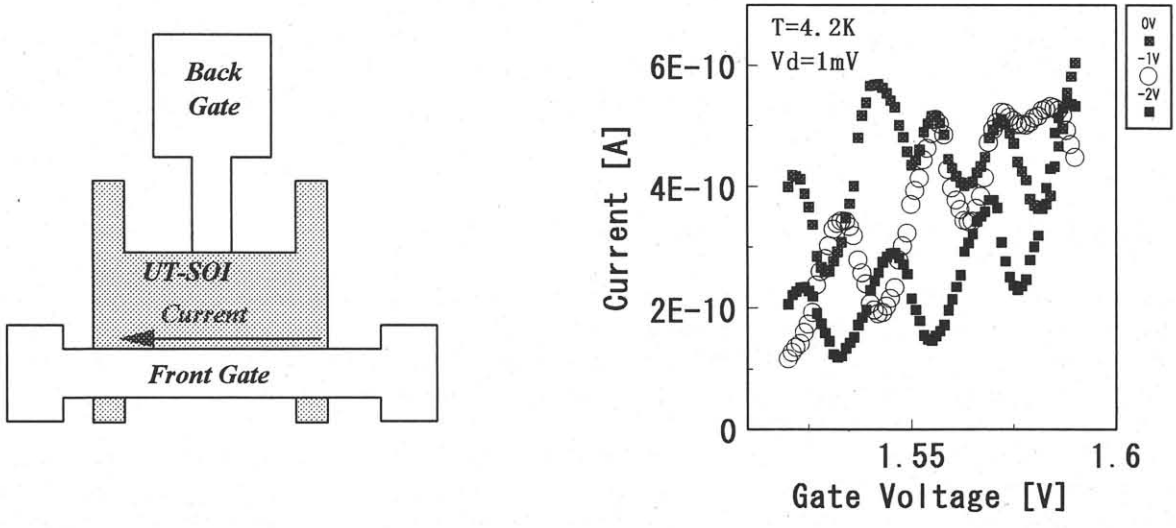


Fig.6 The schematic view of double gate edge quantum wire and the front gate voltage dependence of the current as a parameter of back gate voltage.