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Quantum-Effect Electron Devices Using Metal/Insulator Nanostructures

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Metal($CoSi_2$)/insulator(CaF_2) nanometer-thick heterostructures are grown on a Si substrate, and applied to quantum-effect electron devices. A resonant tunneling transistor was fabricated and a transistor action including negative differential resistance with the peak-to-valley ratio of ~19 was observed at room temperature. A quantum interference transistor utilizing hot electron interference in the conduction band of an insulator sandwiched between metal layers was fabricated and multiple negative differential resistance was observed at room temperature.

1. Introduction

Metal/insulator ultrathin heterostructures are good candidates for high-speed electron devices, because the high carrier density of the metal and the low dielectric constant of the insulator are suitable for size reduction and high-speed operation of devices and integrated circuits(1,2). In addition, due to a very large conduction-band discontinuity at the heterointerface, the interference of the electron wave is expected to become significant in multilayer structures, which may result in high transconductance and multifunctionality of the quantum-effect devices(3,4).

We have been studying epitaxial growth of the metal/insulator heterostructure system(5) and its application to quantum-effect electron devices(6-9). As materials, $CoSi_2$ and CaF_2 have been chosen because they are nearly lattice-matched to Si with mismatches of −1.2% and +0.6%, respectively. In this paper, we describe room-temperature characteristics of metal($CoSi_2$)/ insulator (CaF_2) resonant tunneling transistors and quantum interference transistors fabricated on Si substrate.

2. Epitaxial Growth

In order to create $CoSi_2/CaF_2$ epitaxial mulitlayers, epitaxial growth conditions were studied separately for CaF_2 on $CoSi_2$ and $CoSi_2$ on CaF_2(5). In the case of $CoSi_2$ on CaF_2, the agglomeration of Co on CaF_2 is a critical problem if we use co-deposition of Si and Co with the conventional MBE technique. This problem was overcome by the following two step growth technique: First, flat 4 monolayers of Si were formed on CaF_2 at the substrate temperature Ts= 600℃. Then, 2 monolayers of Co were deposited on the Si layers by the solid phase epitaxy at temperature <100℃. Since the difference of the surface energy between Co and Si is smaller than that between Co and CaF_2, flat 2 monolayers of $CoSi_2$ were grown on CaF_2 with this technique. $CoSi_2$ layers thicker than 2 monolayers were obtained by repeating this process with Si growth temperature of 550℃.

In the case of CaF_2 on $CoSi_2/CaF_2$, Ts must be lower than about 550 ℃ to avoid thermal deformation and agglomeration of $CoSi_2$ layers. We used the partially ionized beam epitaxy to give external kinetic energy for migration to the evapolated particles. CaF_2 was grown on $CoSi_2$ at Ts=450℃ with the acceleration voltage Va=2kV and the ionization current Ie=400mA, at which condition the ionization ratio of the CaF_2 beam was about 2%.

3. Resonant Tunneling Transistor

We fabricated a $CoSi_2/CaF_2$ resonant tunneling transistor shown in Fig.1. The transistor is composed of a few nanometer-thick triple CaF_2 barriers and double $CoSi_2$ wells on n-Si(111). The conduction band offset at the $CoSi_2/CaF_2$ interface is ~15eV and the Fermi level is ~13eV from the conduction band bottom of $CoSi_2$. These values were estimated from the related values of the bulk materials(7). The emitter, base, and the collector electrodes are connected, respectively, to the top $CoSi_2$ layer, one of the $CoSi_2$ quantum wells near the emitter contact layer, and the substrate. Electrons pass through the resonant levels in the two quantum wells from the emitter to collector if these levels are aligned. The alignment and off-alignment between the resonant levels is controlled with the collector-base voltage V_{CB} , and the amount of the electron from the emitter is controlled with the base-emitter voltage V_{BE} . Thus, collector current I_C varies with V_{BE}, and exhibits a negative differential resistance (NDR) with respect to the collector-base voltage, V_{CB}, for constant V_{BE}. As a different case, if the base electrode is connected to the other quantum well, I_C exhibits an NDR with respect to V_{BE} for a constant V_{CB}, which operation is similar to the semiconductor resonant-tunneling hot electron transistor (RHET)(10).

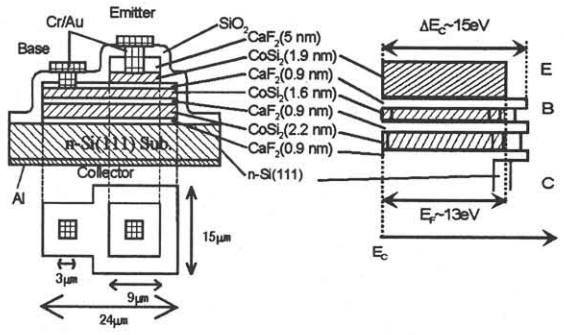

Fig.1 Schematic cross section, top view, and conduction band diagram of fabricated metal/insulator resonant transistor.

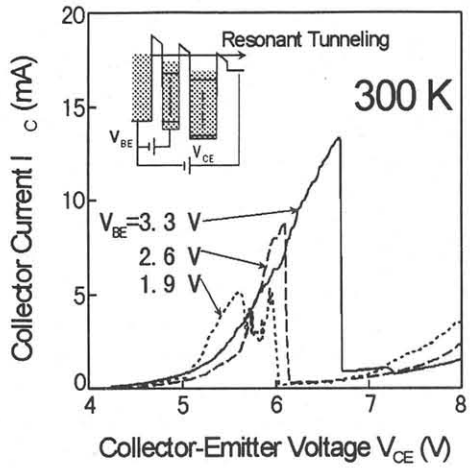

Fig.2 Common-emitter characteristics of metal/insulator resonant tunneling transistor measured at room temperature for different base-emitter voltages V_{BE}.

Figure 2 shows the common-emitter characteristics at room temperature for various values of the emitter-base voltage V_{BE} . Transistor action with NDRs was observed as expected. The peak-to-valley ratio of the NDRs were 13-19. Reduction of the valley current and voltage, which is important in the application to logic circuits, can be done by the suppression of the parasitic elements with the reduction of the device area(8).

4. Device Using Hot Electron Interference

As a quantum effect in metal/insulator system other than the resonant tunneling, the interference of a hot electron wave passing through a metal/insulator/metal structure is also applicable to multifunctional electron

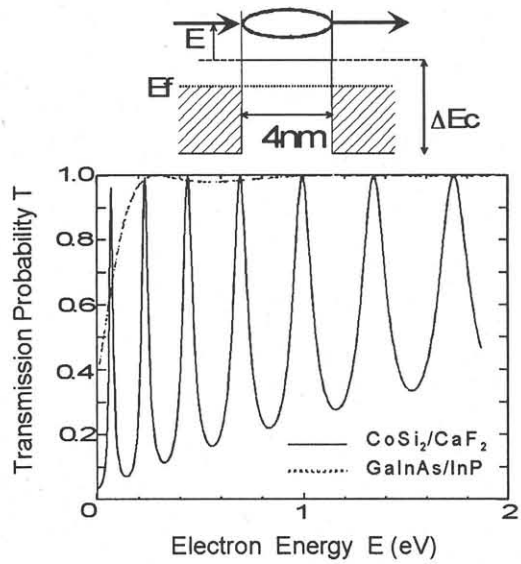

Fig.3 Theoretical calculation of transmission coefficient of $CoSi_2$/ CaF_2/ $CoSi_2$ structure as a function of electron energy measured from insulator conduction band edge. Calculation for semiconductor case (GaInAs/InP/ GaInAs) is also shown by dashed curve.

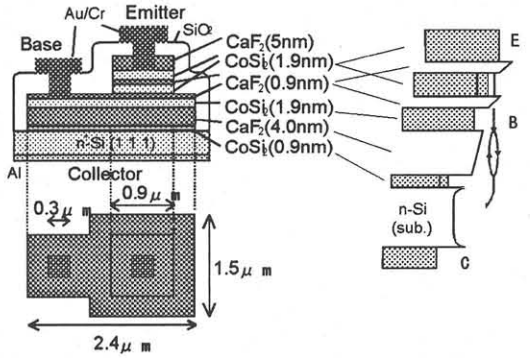

Fig.4 Schematic cross section, top view, and conduction band diagram of fabricated quantum interference transistor.

devices(4). Figure 3 shows theoretical curve of the transmission coefficient modulated due to this interference. This effect is the same as that in a optical Fabry-Pérot interferometer, and is very large in metal/insulator system compared to conventional semiconductor heterostructures due to the large band offset.

To observe this interference, we fabricated a quantum interference transistor structure shown in Fig.4. The transistor is composed of a double-barrier resonant tunneling (RT) emitter ($CoSi_2$/ CaF_2/ $CoSi_2$/ CaF_2 on the top), $CoSi_2$ base layer, CaF_2 collector barrier layer, and a collector region ($CoSi_2$/Si). Hot electrons with collimated energy are emitted from the RT emitter, and injected into the conduction band of the collector barrier interference region. The interference can be observed as the multiple NDRs in the collector current I_C as a function of V_{BE} or V_{CB} . To suppress the collector parasitic resistance and leak current around the device, both of which influence the device characteristics significantly(9), we fabricated small size device (0.3μm design rule) using electron-beam lithography.

Figure 5 shows collector and base currents (I_C and I_B) measured at room temperature as a function of V_{CB} . Multiple NDRs were observed with the voltage interval of ~1.5V. This value agreed reasonably with theoretical calculation (~1V) (9). Stepwise current variation was observed in I_B at the voltages of NDRs in I_C . This may be attributed to additional electrons in I_B at NDR produced by the reflection at the collector barrier interference region.

Although room-temperature operation was obtained, the NDRs are very small due to the leak current, which is still remaining in the thin SiO_2 region close to the device, and also due to the emitter resistance which was produced by sinking of the emitter electrode during the present high-temperature fabrication process of the small-area device. The improvement of the characteristics is possible by optimizing the fabrication process.

5. Conclusions

Quantum-effect devices with metal($CoSi_2$)/insulator (CaF_2) nanometer-thick heterostructures were fabricated on Si substrates, and operated at room temperature. In the epitaxial growth of a $CoSi_2/CaF_2$ multilayer, the two-step growth technique was used for $CoSi_2$, i.e., solid phase epitaxy with the Si layer grown in the first step and Co

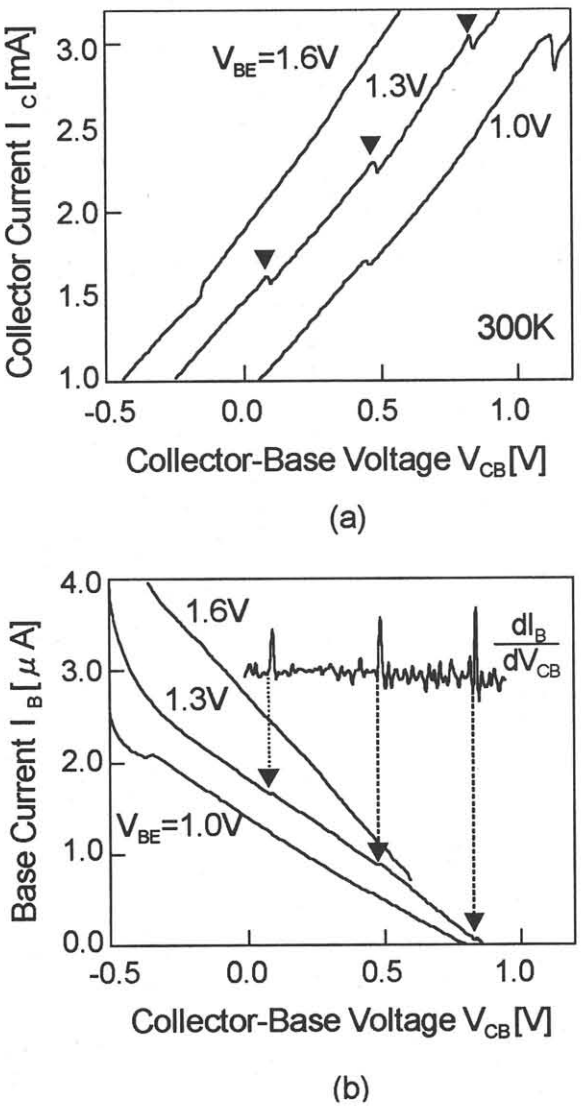

Fig.5 Measured collector current I_C as a function of collector-base voltage V_{CB} for different base-emitter voltages V_{BE}.

deposited in the second step, and a low-temperature partially ionized beam epitaxy was used for CaF_2 A resonant tunneling transistor was fabricated and a transistor action including negative differential resistance with the peak-to-valley ratio of ~19 was observed at room temperature.

A quantum interference transistor utilizing hot electron interference in the conduction band of an insulator sandwiched between metal layers was fabricated and multiple negative differential resistance was observed at room temperature.

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