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Electron Tunneling from a Quantum Wire Formed at the Edge of a SIMOX-Si Layer

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To observe the one-dimensional (1D) subband structure in Si, we fabricated tunnel devices consisting of a 5-nm-thick SIMOX-Si layer, a thin (~2 nm) SiO_2 film (an edge oxide) terminating the Si layer on one side, and a poly-Si electrode covering the edge oxide. We found that the tunneling-current vs. voltage characteristics exhibited a step-like feature at 42 K when the poly-Si electrode was positively biased. The analysis of the tunneling current based on its substrate-bias dependence and measurement-temperature dependence strongly suggests that a quantum wire is formed at the edge of the Si layer due to the band bending and that the observed steps originate from the discrete energy levels of the 1D subbands.

1. INTRODUCTION

Tunneling spectroscopy[1] is a powerful method for investigating the subband structure of a low-dimensional electron system.[2,3] This technique, however, has not yet been applied to the one-dimensional (1D) subband in Si.

To study the 1D electron system in Si, we investigated electron tunneling from the edge of thin SIMOX-Si layers. Figure 1 shows a schematic cross-sectional view of the edge of a SIMOX-Si layer we fabricated. The thin (5-nm-thick) Si layer is terminated by a thin SiO_2 film (an edge oxide). The poly-Si layer covers this structure. When a positive bias is applied to the poly-Si electrode, electrons are induced both in the Si layer and at the edge. Since the edge oxide is much thinner than the SiO_2 films sandwiching the Si layer, the electron density should be higher at the edge than in the Si layer and thus 1D subbands should be formed. The purpose of this study is to observe the 1D subbands by measuring tunneling current flowing through the edge oxide. When the poly-Si bias varies in the positive direction, the band bending at the edge becomes steeper and the energy levels of 1D subbands change their positions with respect to the Fermi level. Therefore, the tunneling current will be modulated when each subband minimum crosses the Fermi level, where an additional subband begins to contribute to the tunneling current.

2. DEVICE STRUCTURE AND FABRICATION PROCESS

The cross-sectional and the plan views of the tunnel device are shown in Figs. 2(a) and 2(b). Electrons are supplied from the n^+ source to the edge via the channel, and then drain into the poly-Si electrode. Hereafter, we refer to the poly-Si electrode as the *front gate* and the substrate electrode as the *back gate*.

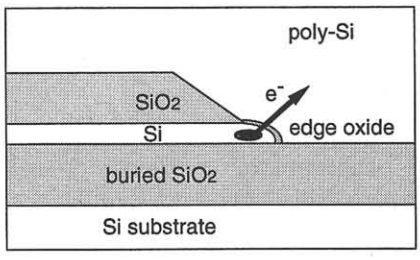

Fig. 1. Schematic cross-sectional view of the edge region. The arrow indicates the direction electrons are emitted.

A Si edge was formed along the [110] direction on a (001)-SIMOX substrate by etching the Si layer using a KOH solution with the front-gate SiO_2 as a mask. The edge of the Si layer was chemically cleaned by H_2SO_4/H_2O_2 and the resultant chemical oxide was removed by an HF solution. Edge oxides 1.7-nm and 2.2-nm thick were then formed in a dry oxygen ambient at 700°C. Next, a phosphorus-doped poly-Si film was deposited and shaped into a gate electrode. We also fabricated devices without the edge oxide, for which the poly-Si film was deposited immediately after the above-mentioned HF treatment. Phosphorous ions were implanted into the source region at a dose of 1 x 10^{16} cm^{-2} and were activated by thermal annealing in a dry oxygen ambient at 800°C. This annealing process at the same time thinned or squeezed the Si layer outside the channel (hatched regions in Fig. 2(b)), preventing the leakage current from flowing through these regions.

TEM images of the edge region with a 2.2-nm-thick edge oxide are shown in Fig. 3. The Si layer is very flat. The root-mean-square value of the thickness fluctuation, obtained using AFM over a scanning area of 1 μm^2, was 0.3 nm. We see in Fig. 3(b) that the Si edge protrudes a little ahead of the front-gate SiO_2. This is because the front-gate SiO_2 receded during the HF treatment.

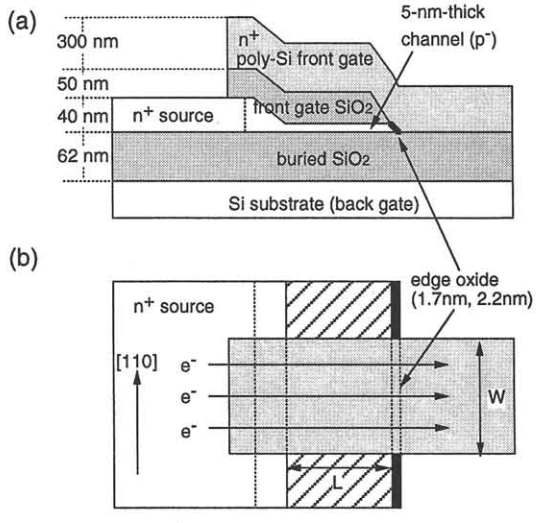

Fig. 2. Cross-sectional view (a) and plan view (b) of the tunnel device. The channel length (L) and the channel width (W) are of the order of micrometers.

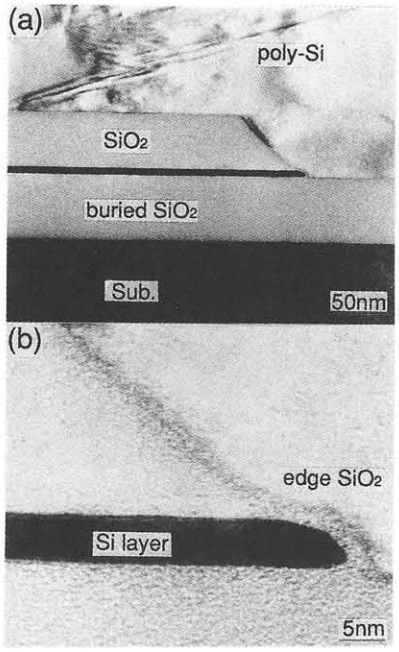

Fig. 3. TEM images of the edge region of the device with a 2.2-nm-thick edge oxide.

3. RESULTS

Two-terminal conductance measurements were carried out in a cryostat system at temperatures ranging from 42 K to over 200 K. An HP4156A semiconductor parameter analyzer was used to apply the voltage and to measure the output current.

Figure 4 shows the current due to the electron emission from the edge as a function of positive front-gate voltage (V_g). The current decreases by several orders of magnitude as the edge-oxide thickness increases slightly, indicating that the tunneling at the edge limits the current for devices with edge oxides. We also confirmed that the current is proportional to the edge width (W). This means that the current flows uniformly through the edges. In Fig. 4, a step-like feature is observed only for devices with edge

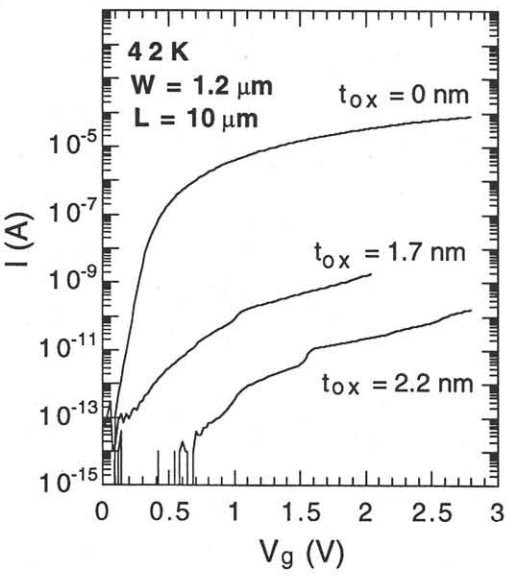

Fig. 4. Current vs. front-gate voltage curves. The source and back-gate voltages were set to be 0 V.

oxides. This is clearly seen in Fig. 5, where the normalized differential conductance, $(V_g/I)(dI/dV_g)$, is shown for the above three devices. Note that the low voltage region has large noise signals because of the low current level. For the device without the edge oxide, the normalized differential conductance has a single peak around $V_g = 0.3$ V. This peak corresponds to the threshold voltage (V_{th}) of the channel, which was confirmed, as shown in Fig. 6, using a MOSFET whose Si layer, front-gate SiO_2 and back-gate SiO_2 have the same thicknesses as those of the tunnel devices. On the other hand, there are several peaks for the devices with the edge oxide. This multi-peak structure is expected to reflect the electronic structure at the edge of the Si layer.

To show that electrons accumulate at the edge due to positive V_g, we present the back-gate voltage (V_b) dependence of the tunneling current in Fig. 7. The $(V_g/I)(dI/dV_g)$ curve shifts towards the negative V_g direction. This is because positive V_b induces additional electrons at the edge, which reduces the V_g required for a given electron density. The amount of the V_g-shift is plotted in the inset of Fig. 7. The slope is 0.022, which is close to the ratio of the edge-oxide thickness to the back-gate oxide thickness (2.2 nm/62 nm = 0.035). This proves that the electron

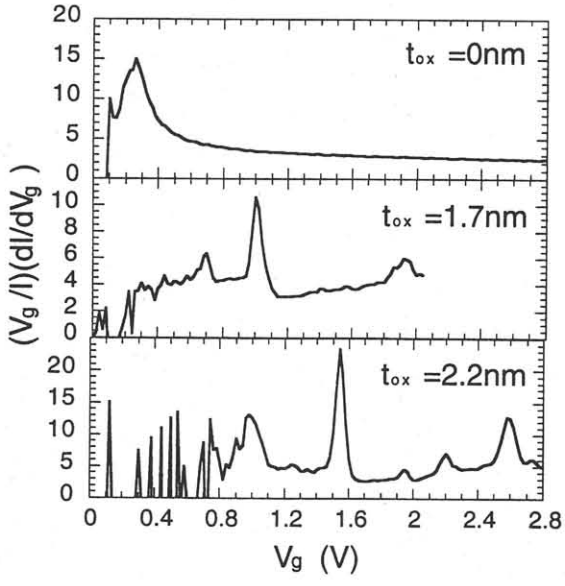

Fig. 5. Normalized differential conductance.

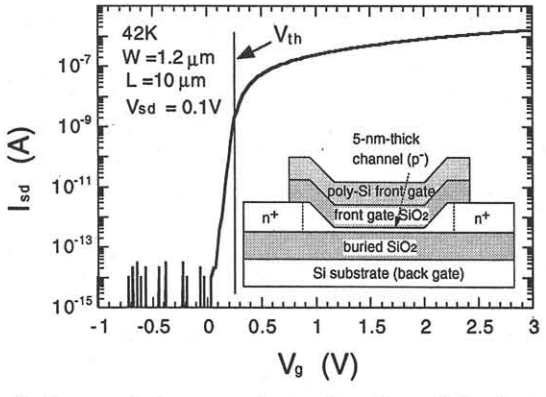

Fig. 6. Source-drain current as a function of the front gate voltage. The source and back-gate voltages were set to be 0 V. Inset is a cross-sectional view of the MOSFET.

density at the edge is approximately determined by the edge-oxide capacitance (C_{edge}) and that the electrons accumulate at the edge. A similar result was obtained for the tunnel device with a 1.7-nm-thick edge oxide.

The measurement temperature dependence of the $(V_g/I)(dI/dV_g)$ curve is shown in Fig. 8. The peak width increases almost proportionally to the temperature, which shows that the width is determined by the Fermi-Dirac distribution and thus corresponds to 3.5 kT. We, therefore, can estimate the energy level spacing between peaks from this figure. By assuming that the change in the Fermi energy (ΔE_f) is proportional to the gate voltage, ΔE_f is given using the change in V_g (ΔV_g) by

$$\Delta E_f = 0.154 \Delta V_g. \qquad (1)$$

According to this equation, the peak spacing for the device with t_{ox} = 2.2 nm (0.3 - 0.5 V) corresponds to 46 - 77 meV in E_f. This indicates that strong confinement occurs at the edge.

4. DISCUSSION

We first evaluate the number of electrons (δn) induced at the edge of the Si layer when the front-gate voltage increases by a peak interval (δV_g). We can express δn as $wWC_{edge}\delta V_g/e$, where w is the width of the edge oxide and wW denotes the area of the edge oxide. Figure 3(b) shows that the value of w is approximately twice as wide as the channel thickness (5 nm) because of the protruded shape of the edge oxide. Setting W = 1.2 μm, t_{ox} = 2.2 nm and w = 10 nm, we obtain δn of 4.6 x 10^2 for δV_g = 0.4 V.

The number of states in a 1D subband (δD) included in a peak interval (δV_g) is expressed as

$$\delta D = \frac{2W g_v \sqrt{2m_D}}{h} \int_0^{\delta V_g} \frac{1}{\sqrt{E}} \frac{dE}{dV_g} dV_g \ . \qquad (2)$$

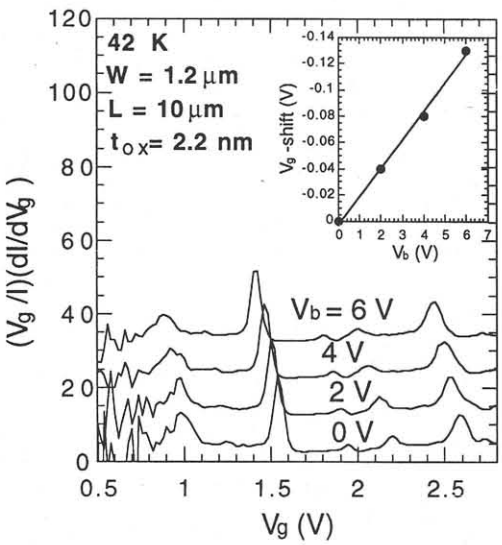

Fig. 7. Back-gate voltage dependence of the $(V_g/I)(dI/dV_g)$ curve. The inset shows the V_g-shift as a function of V_b. The curves are offset vertically by 10.

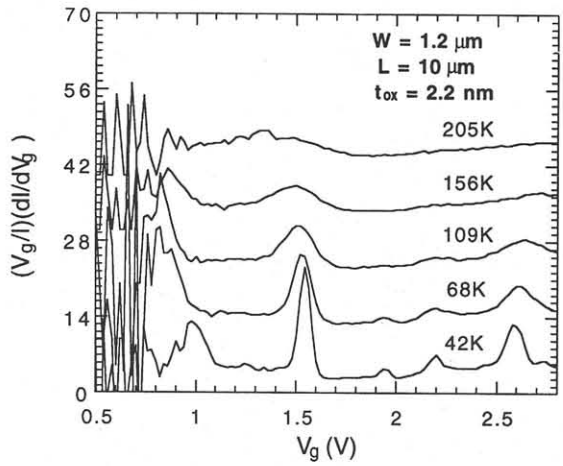

Fig. 8. Measurement-temperature dependence of the normalized differential conductance. The curves are offset vertically by 10.

The δD value should be equal to δn if the 1D subbands predominate in the density of states at the edge of the Si layer. In the present devices, since the edge is aligned to the [110] direction, 1D subbands have two branches, a doubly degenerated one and a fourfold degenerated one.[4] Using Eq. (1), δD is estimated to be 8.5 x 10^2 for the doubly degenerated branch, provided δV_g = 0.4 V. This is of the same order as δn. On the other hand, δD is 3.0 x 10^3 for the fourfold degenerated subbands. This is one order of magnitude larger than δn. This evaluation suggests that the multi-peak structure reflects the discrete energy levels of the doubly degenerated subbands. The situation where the doubly degenerated subbands predominates in the density of states is possible when the electron confinement in the [001] direction (perpendicular to the Si layer in the present case) is stronger than that in the [1$\bar{1}$0] direction (perpendicular to the edge on the (001) plane).[4] A more detailed discussion, however, requires calculation of the potential profile near the edge.

5. CONCLUSION

In conclusion, we have observed steps in the current of electrons tunneling from a Si quantum wire, and our analysis indicates that the steps originate from the discrete energy levels of the 1D subbands.

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