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# Looming Problems and Some Prospective Solutions in Post-0.25 μm Interconnect Technology

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## I. Introduction

In deep submicron ULSI technology, designing and processing a complex system of interconnects are major concerns. Many problems loom ahead as we reach beyond 0.25μm technology. An increasing fraction of signal delay is in interconnect, so that interconnect delay has to be substantially improved in order to meet the expected increase in the chip frequency [1]. At the same time, signal integrity problems such as crosstalk and ground bounce need to be contained within a noise margin that is diminishing each generation. Also, with the number of interconnects well exceeding 10 million, CAD tools which can extract the maximum performance from interconnect systems become essential. This paper reviews some critical issues in post-0.25μm interconnect technology and the prospects for their solutions.

## II. Delay and Signal Noise

The RC delay and the signal noise will be the major factors that dictate the chip performance in deep submicron technologies. The RC delay in the 0.25μm technology already claims 70% of the total delay in the critical nets. This delay component can no longer be improved by increasing the driver size. Instead, interconnect has to be engineered to meet the demand for high speed. Also, the crosstalk noise in the same technology limits the maximum length of an interconnect line to less than 1.0cm [2], which is much shorter than the one perimeter length of a chip. This adds complexity in already complex interconnect routing.

A proper interconnect scaling is important to balance delay and crosstalk [3]. Shown in Fig.1 are constant-delay and constant-crosstalk contours for various interconnect dimensions. Equal metal width and spacing as well as equal metal height and dielectric thickness are assumed for simplicity. For a given delay and crosstalk tolerance, the crossover point of the corresponding contours yields the highest wiring density. The figure implies that delay can be substantially improved by increasing metal pitch, metal height and dielectric thickness simultaneously. In this reverse scaling scheme, the use of the conventional Aℓ/oxide interconnect system is still possible. However, an additional metal layer is required to compensate for the wire density loss. Also, at very high frequencies, the reverse scaling loses its merit because of the skin effect.

Another approach to reduce RC delay is to employ Cu metallization to lower resistance and low-ε dielectric to lower capacitance. Approximately 30% resistance reduction with Cu and 40% capacitance reduction with an organic dielectric are typically expected. However, the improvement of speed at the circuit level by these new materials still remains marginal at around 10% as shown in Table 1. Instead, the Cu lines should be admitted to the deep submicron interconnect system not because of improvement in delay but because of its superior electromigration characteristics and improvement in IR drop. The low-ε dielectrics, on the other hand, will suppress crosstalk in short lines. But long lines will still be plagued with crosstalk noise because the ratio of capacitive coupling to ground and coupling to signal still remains unchanged with the new dielectric materials.

A more effective method to overcome the delay and crosstalk problems is an insertion of repeaters. Long lines are divided into two or more segments, and inverters are added between the segments. In Fig. 2 delay and crosstalk as a function of the number of inserted repeaters are presented. With an appropriate number and placement of repeaters, 25% and 50% reduction in delay and crosstalk, respectively, can be obtained. However, an increasing number of lines will start to require repeaters as the chip frequency increases. Therefore, an efficient repeater insertion and routing algorithm in the CAD tools becomes essential to take advantage of this approach. Wire sizing can be concurrently performed with the buffer insertion. It scales down line width as the distance to the driver increases and effectively achieves a lower RC constant. But its impact on delay is secondary as compared to that of buffer insertion.

With a rapid increase both in the clock rate and the degree of device integration, ground bounce will also be a critical issue. A generous amount of power and ground lines will reduce this concern, but at the cost of signal routing area.

At the clock rates exceeding 1GHz, the inductive coupling in interconnect will start to generate noticeable signal noise. The inductive coupling cannot be minimized by means of new materials or scaling. It rather depends on routing topology. A dense power and ground array can significantly suppress both self-inductance and mutual inductance by ensuring the shortest current loop possible. Similarly, an insertion of a repeater shortens the current loop and reduces the inductive noise.

## III. Interconnect Characterization and Modeling

Interconnect characterization and modeling will be an integral part of performance enhancement in deep submicron interconnect technology. They ensure that the impact of new materials, repeaters, and wire sizing are fully translated into performance improvement at the chip level.

Accurate extractions of interconnect resistance and capacitance values are critical in timing and signal integrity analysis. The extraction results from CAD tools are generally accurate, provided interconnect geometry is precisely described in their input files [5]. However, a detailed account of interconnect geometry is made difficult because of large line width and dielectric thickness variations in deep submicron interconnect. One way to improve the accuracy of delay and crosstalk analysis is to generate a heuristic database for various interconnect geometries [6]. But this approach may become impractical since the database needs to be extremely large as the number of metal layers increases.

Realistic estimation of interconnect capacitance and resistance variation due to process variations is also important; underestimation can produce false switching whereas overestimation will sacrifice performance. Assumption of the worst-case line width, line height, and dielectric thickness yields a delay variation that is too pessimistic. A more statistically-based worst case estimation [7] can tighten the 3-σ delay variation by more than 50%.

## IV. Conclusion

Some critical issues in post-0.25μm interconnect technology were discussed. No single technique will solve the numerous problems we face. Simultaneous advancement in the interconnect process, characterization, modeling and design is essential. Also, these technologies must be mated with CAD tools since the number of interconnects is expected to increase drastically over the next generations.

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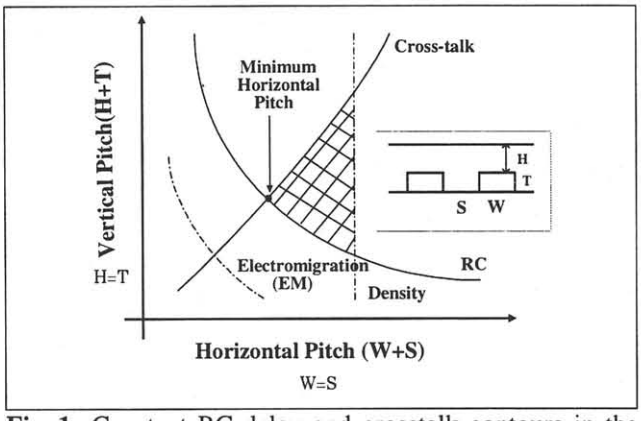


**Fig. 1** Constant RC delay and crosstalk contours in the interconnect scaling space. The allowed region (fast delay, small crosstalk, and higher density) is shown as a shaded area.

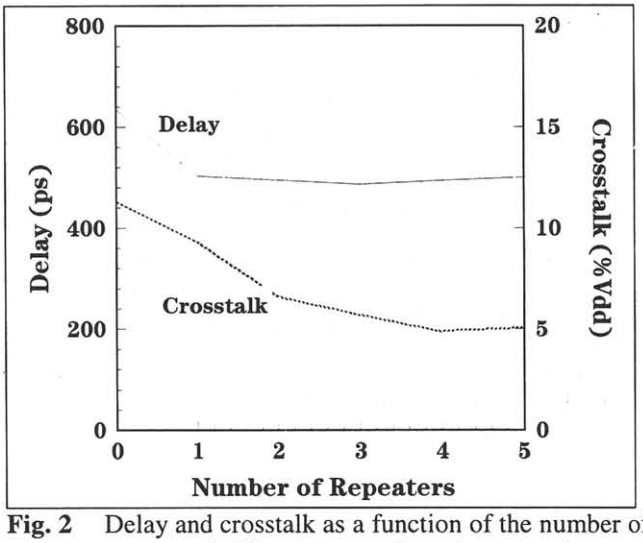


**Fig. 2** Delay and crosstalk as a function of the number of repeaters. The repeater insertion can decrease delay and crosstalk by 25% and 50% respectively.

| Size | Nominal | Low-ε | Cu |
|---|---|---|---|
| 128x64 | 1.02ns | 0.94ns (8.2%) | 0.98ns (3.8%) |
| 256x64 | 1.48ns | 1.33ns (10.2%) | 1.41ns (4.9%) |
| 512x64 | 2.57ns | 2.24ns (12.7%) | 2.38ns (7.3%) |

**Table 1** Cache RAM access time with Low-ε dielectrics and Cu. The numbers in parentheses represent improvement from the nominal case.